# CMOS Digital Isolators Supersede Optocouplers in Industrial Applications

## Introduction

Isolation circuits designed to withstand the rigors of industrial environments are the focus of this white paper. Industrial electronic equipment commonly uses galvanic isolators to protect systems and users from potentially hazardous voltages. It is well known that industrial equipment must operate reliably in the harshest environments, where strong electromagnetic fields, surges, fast transients, and high noise floors are the norm. This environment presents challenges for designing reliable isolation circuits that deliver error-free operation over long equipment lifetimes.

Over the last four decades, optocouplers have been the "default" signal isolation device, but recent breakthroughs in silicon isolation technology have spawned smaller, faster, and more reliable and cost-effective solutions that have already begun supplanting optocouplers in many end applications. Of the competing silicon isolators currently on the market, the Silicon Labs *CMOS digital isolator* family is the most advanced, offering best-in-class timing performance, electromagnetic interference (EMI) and external field immunity, power consumption, size, and cost. This white paper discusses industrial isolation issues and ways RF isolation technology can be applied to increase system robustness and performance.

## RF Isolator and Optocoupler Basics

Figure 1 shows top-level block diagrams of an optocoupler and the CMOS digital isolator. As shown in Figure 1a, the optocoupler is a hybrid assembly having a light-emitting diode (LED) that emits light when forward biased, with brightness being proportional to LED forward current. Emitted light passes through an optically transparent insulating film (or dielectric), striking a photo detector and causing a current flow that biases the output transistor on. When LED forward current no longer flows, light emission ceases, and the output transistor turns off.
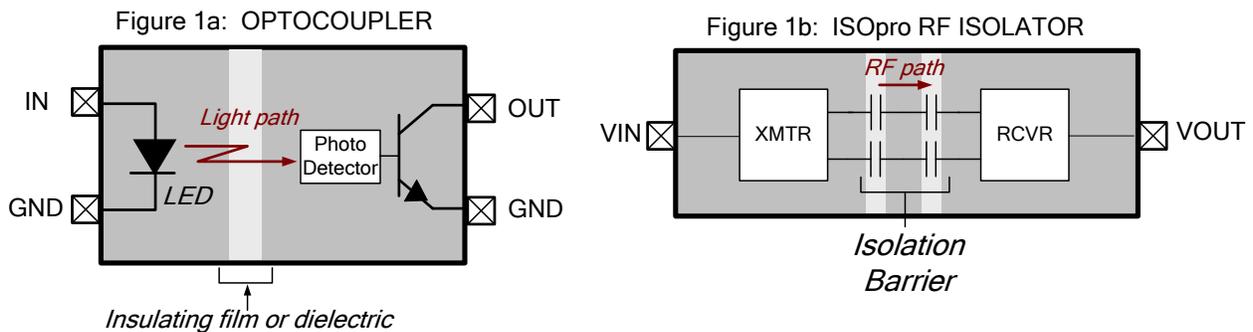


**Figure 1. Basic Operation of Optocoupler vs. CMOS Digital Isolator**

The basic operation of the CMOS digital isolator is analogous to that of the optocoupler, except that an RF carrier is used instead of light (Figure 1b). The CMOS digital isolator consists of two identical semiconductor dies connected together within a standard IC package forming an RF transmitter and receiver separated by a differential capacitive isolation barrier. Data is transferred from input to output using simple on/off keying (OOK). When VIN is high, the transmitter generates an RF carrier that propagates across the isolation barrier to the receiver. The receiver asserts logic 1 on VOUT when sufficient in-band carrier energy is detected. When VIN is low, the transmitter is disabled, and no carrier is present. The receiver, therefore, detects no in-band carrier energy and drives VOUT low.

## Device Construction

While the basic operating principles of both the CMOS digital isolator and optocoupler are similar, the physical implementation of each is quite different. An X-Ray view of a single-channel optocoupler is shown in Figure 2a. The optocoupler's hybrid construction attaches the LED and output die to a split lead frame. These two dies are separated by a physical gap containing a transparent insulating shield intended to reduce parasitic input/output coupling capacitance. The optocoupler's isolation breakdown voltage is determined primarily by the package plastic mold compound. Note that optocoupler cost and complexity directly increase with channel count, making higher channel count optocouplers more difficult to realize than their monolithic silicon counterparts.
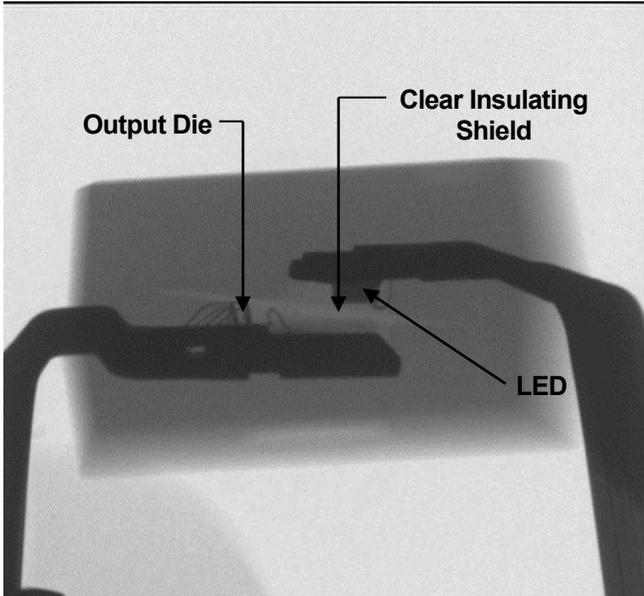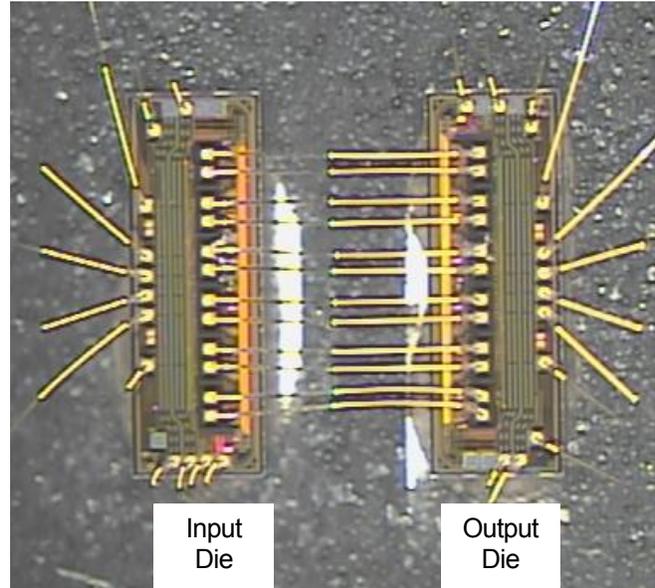


**Figure 2a.  Optocoupler Assembly X-Ray**



**Figure 2b.  Decapsulated 6-Channel CMOS Digital Isolator**

A decapsulated view of the six-channel CMOS digital isolator is shown in Figure 2b. Standard complementary metal oxide semiconductor (CMOS) process technology and standard IC packaging are used throughout. Each of the two dies contain six complete isolator channels, where each channel consists of a transmitter, differential isolation barrier, and receiver circuit. When the two dies are connected, the capacitive isolation barrier of each die is in series with the other, doubling the channel breakdown voltage for greater safety margin.

Unlike the optocoupler, each CMOS digital isolator channel occupies little die area, making possible cost-effective, high-channel-count isolators. Additionally, monolithic semiconductor process technology enables CMOS isolation technology to be combined with other semiconductor functions and processes to create highly-integrated products with built-in isolation, such as isolated analog data converters and communication transceivers. These integration advantages enable a broader, more comprehensive isolation product roadmap than the optocoupler.

**Process Technology**

The CMOS process technology used in the fabrication of the CMOS digital isolator is pervasive and available from virtually all mainstream semiconductor foundries. CMOS technology is used in digital products, such as microprocessors, microcontrollers, and static RAM, and in analog products, such as image sensors, analog data converters, and integrated communication transceivers. CMOS is best known for high noise immunity, low static power consumption, high reliability, and economy. Over the years, CMOS process geometries have shrunk continuously, enabling new products with increased functional capabilities and lower cost and power consumption. The combined electronics industry learning and production of CMOS far exceeds that of the GaAs-based technologies used in optocouplers.
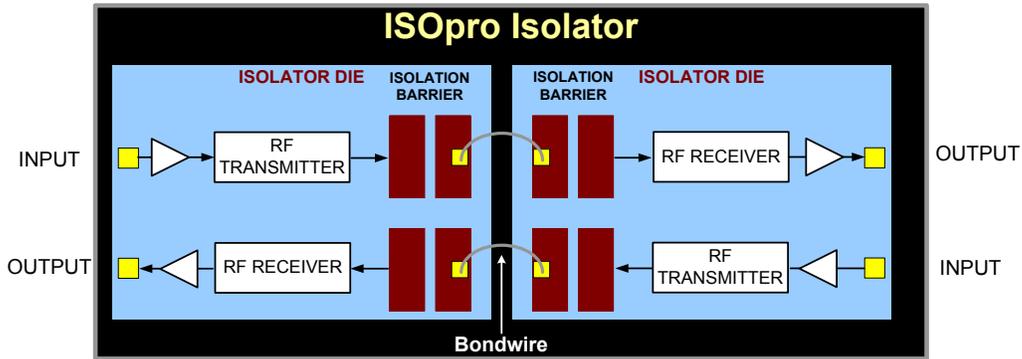


**Figure 3. CMOS Digital Isolator Channel Block Diagram (View from Top of Die)**

**Signal Path**

The CMOS digital isolator's differential capacitive isolated signal path is diagramed in Figure 3 above. Isolation capacitor plates are fabricated on the top layers, and buried metal layers and standard process oxides are deposited between the capacitor's lower plates providing insulation. Active support circuitry, such as the transmitter and receiver, are located on the same die but away from the isolation capacitors. The signal isolation path is completely differential from transmitter to receiver for maximum common-mode rejection. As shown in Figure 4, the receiver's active differential gain causes it to recognize only the *difference* between its V+ and V- input signals. Any common-mode voltages, such as RF interference or common mode transients, appear on both the V+ and V- inputs and are cancelled at the differential input as shown in Figure 4.
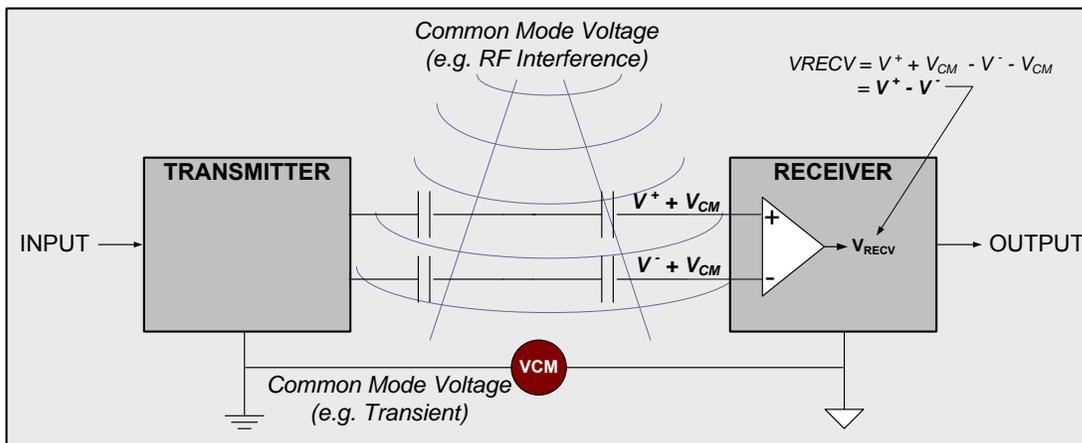


**Figure 4.  Single-Channel Representation of CMOS Isolator Differential Signal Isolation Path**

**System Considerations**

Regardless of implementation, isolators must meet safety standards for robust galvanic isolation. They must also be reliable enough to outlast the equipment in which they are installed, which, in the industrial world, can mean decades of use. Designers must ensure that isolation circuits can withstand electrical stresses that can cause physical damage and reject data-corrupting noise from any number of sources. Therefore, the designer must carefully consider key isolator operating parameters, such as common-mode transient immunity, key timing parameters, such as propagation delay and pulse width distortion, and field-related specifications, such as EMI and RF susceptibility. Likewise, continuous working voltage and mean time-to-failure (MTTF) are important indicators of device service life.

## High Voltage Insulation Reliability

Insulation reliability directly affects the isolator's ability to safeguard against user exposure to high voltage and is of paramount importance. The insulator is the "heart" of the isolation barrier and key to maintaining system safety. It is very important that the insulation be uniform, with no voids that can cause a localized breakdown. Insulator uniformity is a function of insulator material and the fabrication process.

The dielectric strength of the optocoupler's injection-molded plastic compound can vary by as much as 300% due to voids created during fabrication. In contrast, the CMOS digital isolator uses semiconductor oxide layers for its primary insulator. The CMOS oxide deposition process is very tightly controlled and highly uniform, and the resulting variation in dielectric strength is only 20%. Each oxide layer has a breakdown voltage of 500 $V_{ACRMS}$ per micron (millionth of a meter). Higher voltages (e.g. 5 $kV_{ACRMS}$) are implemented by simply stacking oxide layers during wafer fabrication. The result is a higher absolute maximum breakdown voltage in a substantially smaller size compared to optocouplers and insulator reliability that is independent of the packaging process.
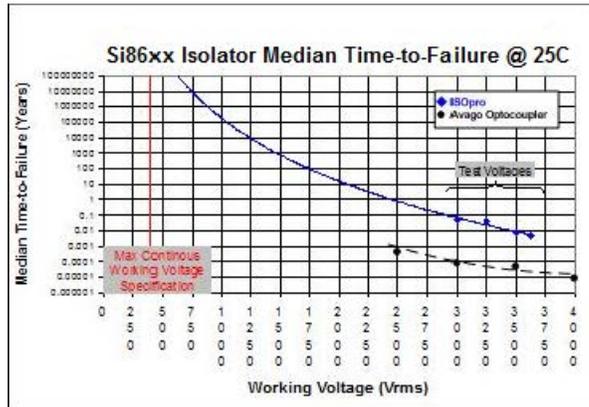


**Figure 5.  CMOS Digital Isolator vs. Optocoupler Mean Time to Failure**

Figure 5 compares the median time-to-failure of the CMOS digital isolator versus an optocoupler. Both devices were measured on the same equipment and under the same conditions. As shown, the extrapolated median time-to-failure for a 2.5 $kV_{ACRMS}$, 6-channel CMOS digital isolator trends toward $1 \times 10^8$ years at 25 °C with 500 $V_{DC}$ applied.

## Safety Certifications

International safety standards provide test methodologies and guidelines to ensure end-equipment safety from electrical shock, mechanical hazard, and fire and electromagnetic interference. The

component-level international safety standards for optocouplers and other isolators (including CMOS digital isolators) are summarized geographically in Table 1.

**Table 1. International Certification Agencies and Standards (Optocoupler Components)**

| International | Europe | U.S. | Canada | Germany |
|---|---|---|---|---|
| IEC | CENELEC | UL | CSA | DIN/VDE |
| IEC 60747-5-2 | EN 60747-5-2 | 1577 | Component Acceptance Notice #5A | DIN EN 60747-5-2 |

Isolator classifications include "Basic" and "Reinforced". Basic isolation is intended to provide a single-level of protection against electrical shock only and cannot be considered failsafe. While these devices are accessible to a user, they must be contained within the system. Basic isolation devices are 100% safety tested at 2.5 kV$_{ACRMS}$ for a period of 1 minute and, typically, have a minimum creepage of 3.2 mm. Reinforced isolation provides two levels of protection, making these devices failsafe and allowing user access. These devices are 100% safety tested at 5 kV$_{ACRMS}$ for a period of 1 minute and typically provide a minimum creepage of 6.4 mm. Note that the exact creepage distance and rated isolation voltage requirements vary from one system to another according to the system's specifications and targeted environmental operating conditions (pollution degree).

Certification testing involves subjecting the isolator component to various stresses as prescribed by test standards while monitoring the device under test for failures that could compromise safety.

**Table 2. Test Voltages per IEC60950**

| Grade of Insulation | Points of Application (where appropriate) | | |
|---|---|---|---|
| | PRIMARY CIRCUIT to BODY PRIMARY CIRCUIT to SECONDARY CIRCUIT between parts in PRIMARY CIRCUITS | | |
| | WORKING VOLTAGE | | |
| | U ≤ 184 V peak or d.c. | 184 V < U ≤ 354 V peak or d.c. | 354 V < U ≤ 1.41 kV peak or d.c. |
| | Test Voltage, Volts RMS | | |
| Functional | 1,000 | 1,500 | See IEC60950 Va in Table 5B, part2 |
| Basic, Supplementary | 1,000 | 1,500 | See IEC60950 Va in Table 5B, part 2 |
| Reinforced | 2,000 | 3,000 | See IEC60950 Va in Table 5B, part 2 |

Table 2 is an excerpt from the electrical strength test prescribed by IEC60950. The test voltages shown assume homogeneous joined package surfaces, such as molding compound only. However, different materials are used in the isolation barrier of both optocouplers and CMOS digital isolators.
For example, the CMOS digital isolator uses silicon dioxide as the primary insulator and plastic mold compound as its secondary insulator. This type of non-homogenous, joined construction is referred to as "cement joint" and requires the certification agency to *proof test* the isolator by increasing the test voltages of

Table 2 by a factor of 1.6. For example, reinforced components that support a peak or dc working voltage of 354 V must tolerate a 4,800 $V_{ACRMS}$ dielectric withstand potential for 1 minute to pass agency certification for a rated voltage of 4,800 $V_{ACRMS}$. In addition, the manufacturer's production test for this isolator must include testing each component at 120% of its rated value for 1 second. Therefore, the 354 V isolator referenced above would be production tested for 1 second at 5,760 $V_{ACRMS}$ (4,800 Vrms x 1.2) to ensure its integrity.

**Operating Power**

At a minimum, optocouplers require current to bias the LED and some form of bias on the output side. The total input plus output current varies widely, depending on the type of optocoupler. When forward biased, the optocoupler LED is low-impedance, and device power consumption increases with LED forward current, which can range from 1 mA to over 15 mA. In some cases, the LED may require an external driver, further decreasing system efficiency while increasing BOM complexity and cost. The optocoupler output impedance can be low or high depending on its architecture. Most low-cost optocouplers have a simple transistor output that is high-impedance when LED forward current is at zero and relatively lower impedance when LED forward current is in its specified operating range. Other (usually higher speed) optocouplers have an active photo coupler and output driver that requires an external bias voltage. Such devices have low output impedance but at the expense of increased total operating current, which can range from 15 mA to over 40 mA.

Compared to optocouplers, CMOS digital isolators offer significantly higher operating efficiency, consuming approximately 1.7 mA per channel at 10 Mbps at VDD = 5.0 V with a 15 pF load. Its high-impedance input buffer consumes only microamps of leakage current while its 50 $\Omega$ CMOS output driver can source or sink 4 mA. The bulk of the CMOS digital isolator's power savings results from the use of an RF carrier instead of light, eliminating the power-hungry LED. Losses in the isolation path are minimized by the isolation capacitor structures, which are optimized for robust data transfer and minimum power loss. The CMOS digital isolator's power dissipation remains relatively flat and substantially less than that of the optocoupler. The only noteworthy contributor to increased supply current is increased data rate, yet even this increase is relatively shallow as shown in Figure 6.
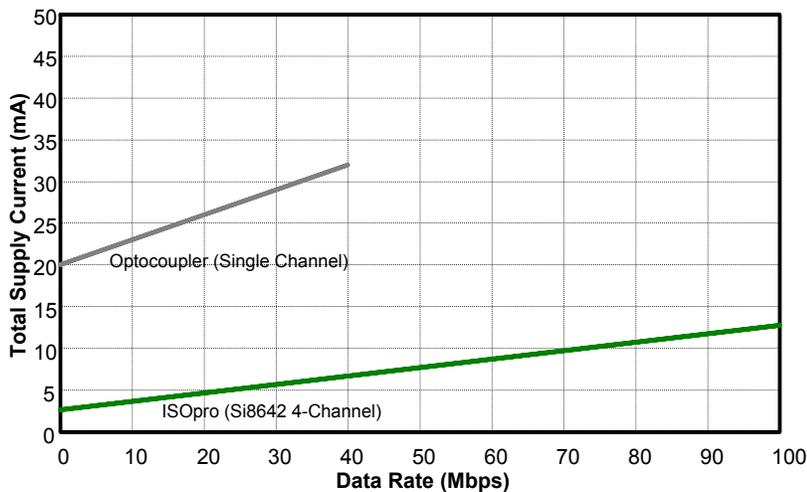


**Figure 6. Current Consumption of CMOS Digital Isolator vs. Optocoupler Operating Stability**

Given the typical service life of industrial equipment, long-term reliability and consistent performance are paramount concerns for the system designer. Optocoupler timing parameters (e.g. propagation delay and pulse width distortion) can change with three variables: LED wear-out, LED current, and operating temperature.

One of the key optocoupler wear-out mechanisms is *LED light output* (LOP), a material-based phenomenon that causes the LED to lose brightness over time. Lower emission decreases the signal seen by the

photodetector, negatively impacting optocoupler timing and output impedance characteristics. Figures 7a and 7b show manufacturer's LOP data based on normalized light output over a period of 10,000 hours for LEDs made from both Gallium Arsenide Phosphide (GaAsP) and Aluminum Gallium Arsenide (AlGaAs). Light output degradation typically worsens with increasing temperature and increasing LED current. In the worst case, the light output can fall below the minimum value required for proper device operation.



a. GaAsP LED

b. AlGaAs LED
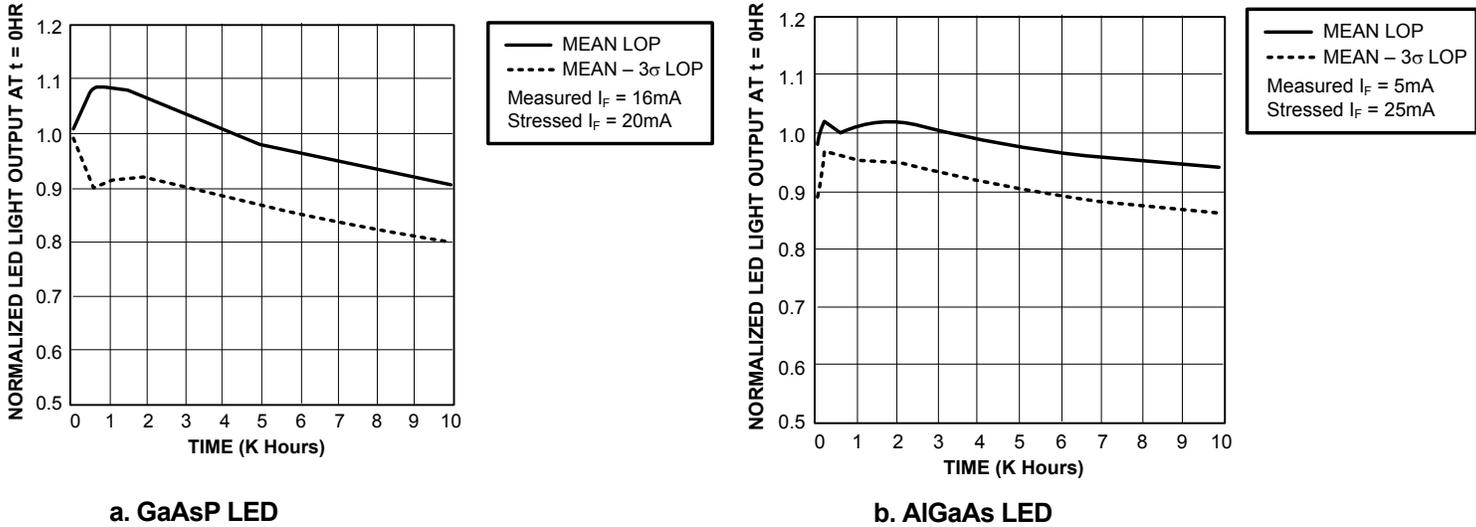
**FIGURE 7a and 7b: Optocoupler Manufacturer's LOP Test Data**

As shown, LOP can change nominal light output by as much as 20% (Figure 7a) causing significant changes in operating characteristics. Moreover, since the rate of LOP degradation is partially related to LED current, the system designer must take into account the effects of LOP when choosing the LED forward current operating range. For example, lower LED drive current can be traded for longer device service life but lower common-mode transient immunity (CMTI). Conversely, higher LED drive current can be traded for improved CMTI but shorter optocoupler service life. Silicon Labs' CMOS digital isolators do not suffer from any wear-out mechanisms when used within rated operating conditions.

**Timing Characteristics**

Timing specifications are important in digital isolator applications to ensure proper and consistent system operation. Figure 8 compares the propagation delay characteristics of the 10 Mbps CMOS digital isolator with those of a competing digital optocoupler. Propagation delays were measured with different LED currents, both with and without a "peaking" capacitor.

Note: The peaking capacitor in this case is 20 pF in parallel with the LED current limit resistor. This capacitor momentarily increases LED current during turn-on and turn-off for faster optocoupler response.

In Figure 8, curves B and C show propagation times for LED currents of 0.5 mA and 1.0 mA and no peaking capacitor. As shown, a 0.5 mA decrease in LED current results in a 50% increase in propagation time (80 ns to 120 ns) at 20 °C, demonstrating the large timing variations that result from changes in LED current and/or wear-out. Propagation delay is not symmetrical; curve A shows a high-to-low transition fastest propagation time of roughly 35 ns at 20 °C, but the low-to-high transition is twice the propagation delay time. Therefore, a system using this component must take into account these asymmetric delays and provide additional timing margin. While this example demonstrates the changes in propagation

time, it is important to note that other optocoupler timing parameters, such as pulse width distortion, channel-to-channel matching, rise and fall time, etc., will follow the same trend because all timing behavior, including LOP effects, is related to LED emission.
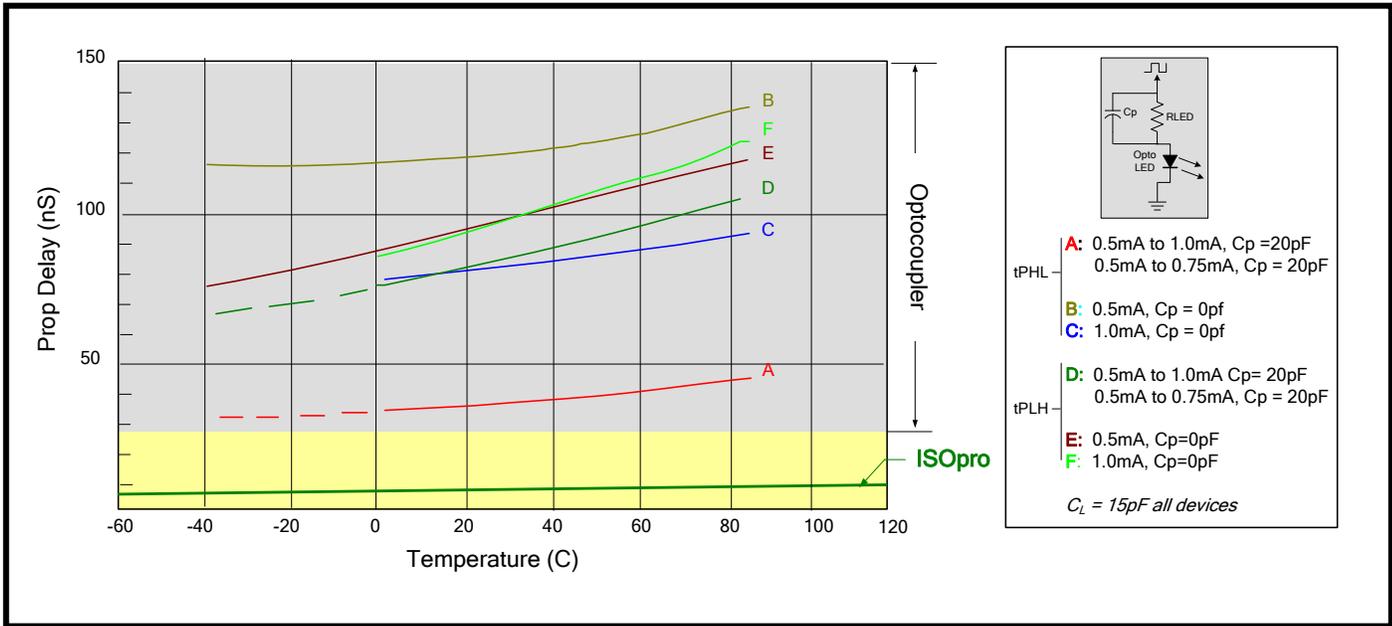


**Figure 8. Optocoupler vs. CMOS Digital Isolator Propagation Delay**

Unlike the optocoupler, the CMOS digital isolator's timing parameters are a function of internal precision timing circuits and fixed propagation delays within its signal path. All timing parameters vary only slightly with changes in VDD, and all remain flat over temperature. For example, rise and fall times vary by only 1 ns across temperature and supply voltage, and worst-case propagation time is approximately 9 ns at 120 °C. Table 3 shows the operating characteristics of a 50 Mbps optocoupler compared to the CMOS digital isolator.

**Table 3. Characteristics of CMOS Digital Isolator vs. Optocoupler**

| Product | Channels | Operating Temp Range (Deg. C) | Supply Voltage (V) | Max Supply Current (input + output) (mA) | Max Prop Delay Time (ns) | Minimum Pulse Width (ns) | Maximum Data Rate (Mbps) | Pulse Width Distortion (ns) | Prop Delay Skew (ns) | Output Rise Time (ns) | Output Fall Time (ns) | Channel-to-Channel Skew (ns) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISOpro | 4 | -40 to +125 | 2.7 to 5.5 | 7 | 10 | 6 | 150 | 1.5 | 2 | 4 | 4 | 0.5 |
| Optocoupler | 1 | -40 to +85 | 4.5 to 5.5 | 17.5 | 22 | 20 | 50 | 2 | 16 | 8 | 6 | 20 |

**Common-Mode Transient Immunity (CMTI)**

Common-mode transients are one of the leading causes of data corruption in isolation applications. CMTI is commonly measured in kV per microsecond and refers to the ability of an isolator to reject noise that is present between the isolator input and output. Figure 9a shows an optocoupler subjected to common-mode noise, $V_{CM}$. As $V_{CM}$ changes due to fast transients, iLP and iLN either aid or oppose the LED current, causing

a momentary change in LED light emission, often in spite of the detector shield added by manufacturers to reduce parasitic capacitive input/output coupling.
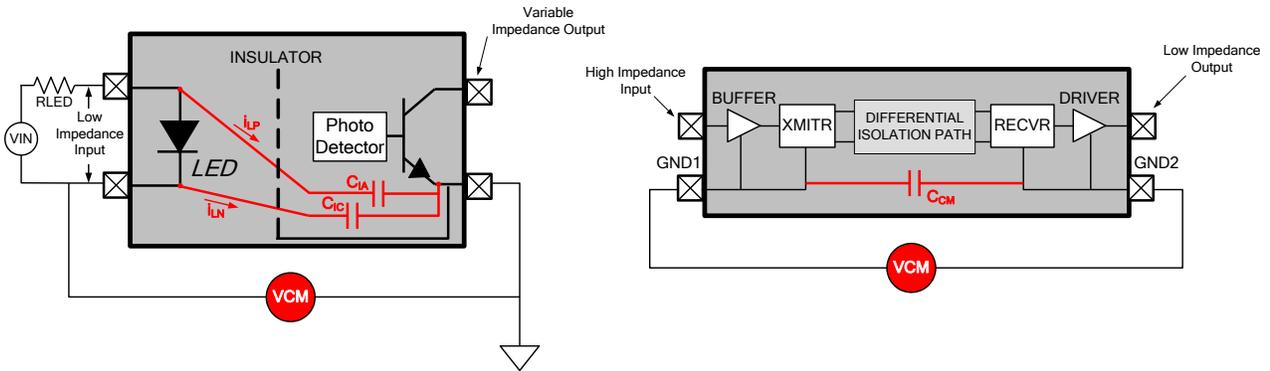


**FIGURE 9a. Optocoupler Equivalent Circuit**          **FIGURE 9b. CMOS Digital Isolator Equivalent Circuit**

The optocoupler parasitic coupling between grounds is typically in the range of tenths of picofarads (e.g. 0.6 pF for the Avago HCPL-0703), which greatly decreases CMTI. Some degree of CMTI improvement can be obtained using the "quasi-differential" drive shown in Figure 10, where LED current-limiting resistors are placed on both sides of the LED, each having half the value of $R_{LED}$ in Figure 9.
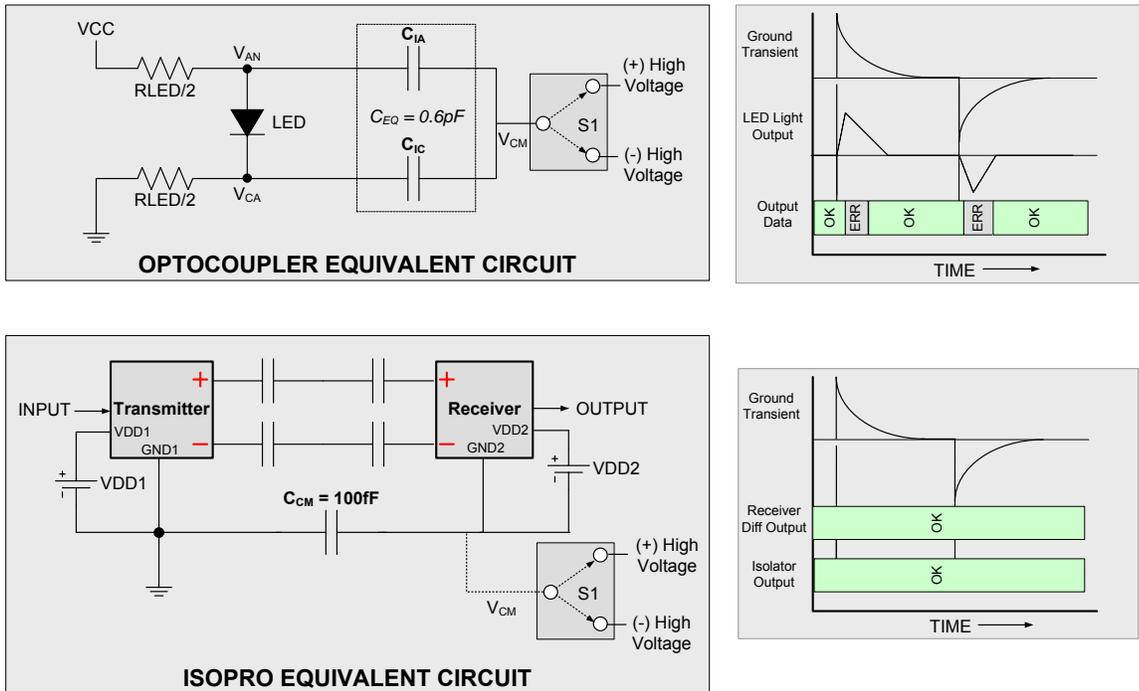


**Figure 10.  Common Mode Transient Models for Optocoupler and CMOS Digital Isolator**

As shown in the optocoupler timing diagram of Figure 10, a positive-going ground transient on the optocoupler's right-side ground (with respect to the left-side ground) causes a momentary increase in

LED current. This LED "glitch" can cause data errors, depending on the magnitude of the transient and the amount of parasitic coupling present in the optocoupler. For example, a 0.6 pF coupling may be sufficient to erroneously turn on the LED momentarily when it should remain off. Likewise, a negative-going transient can erroneously turn off the LED when it should remain on. The inherently low CMTI of optocouplers is discussed at length in application manuals issued by optocoupler manufacturers, some of which recommend over-driving the LED while in the on state and reverse-biasing the LED while in the off state when operating in high common-mode environments. While this technique is effective, it increases LED power dissipation and hastens the wear-out due to LOP. In any case, the parasitic coupling is unavoidable and degrades optocoupler CMTI performance.

The bottom graphic of Figure 10 shows the CMOS digital isolator with its common-mode voltage, $V_{CM}$, and its 100 femtofarad input-to-output capacitance ($C_{CM}$), which is six times smaller than that of the optocoupler. Its fully-differential isolation path rejects common-mode voltages, and the high selectivity of the receiver rejects all but the carrier frequency for even greater noise immunity. For these reasons, the CMOS digital isolator has a *typical* CMTI of 60 kV/µs, substantially higher than most optocouplers using external components to improve CMTI.

**Electromagnetic Interference (EMI)**

EMI refers to any electromagnetic disturbance that disrupts or otherwise interferes with the effective performance of authorized electrical equipment. As it pertains to isolators, radiated and conducted EMI is generally the product of high-frequency switching circuits (and their harmonics) that couple into other circuits and/or the environment. Radiated EMI is analogous to broadcast in that it travels from transmitter to receiver through free space, whereas conducted EMI travels along a conductor. The FCC sets limits for both conducted and radiated EMI, and all devices in a given class must comply with these standards.


Specifications published by various agencies place limits on conducted and radiated EMI. One of the more common specifications is FCC Part 15, which covers circuit assemblies used in or near the home. Testing to this specification is conducted in an open-air environment using a 10 meter antenna positioned approximately 5 meters above the ground plane.

Another specification, SAEJ1752-3, is more IC-centric in its test methodology and recommends mounting the IC to be tested on a small circuit board and measuring the radiated emissions from the board while operating within the actual application environment. For this test, radiated EMI limits for various frequency bands are specified by CISPR-25, a subset of automotive EMI specification SAE J1113.

EMI testing to FCC Class B Part 15 was performed using two test boards, each containing a socketed 6-channel CMOS digital isolator with all inputs tied high to maximize emissions from the internal transmitters (i.e. 12 channels switching at full speed on two socketed boards). The CMOS digital isolator passed FCC Class B Part 15 in spite of the use of the sockets, which increase EMI emissions. The CMOS digital isolator achieves low EMI operation primarily through a combination of the field-cancelling internal differential signal path, the sizing of the isolation capacitors, and the design of the low-power main oscillator. The EMI plots are available from Silicon Laboratories upon request.

**RF Immunity**

RF immunity is the ability of the isolator to reject strong local electromagnetic fields, thereby maintaining error-free data transfer. Intuitively, one might assume that ambient RF fields would interfere with the CMOS digital isolator's internal RF data transmission. However, the CMOS digital isolator demonstrates an extremely high degree of external RF noise rejection by virtue of its design.

Local fields induce common-mode voltages within the CMOS digital isolator's internal signal path that are rejected by a combination of the CMOS digital isolator's differential isolation signal path and high receiver selectivity. Signal levels on each side of the CMOS digital isolator's internal differential signal path are tightly matched, causing common-mode voltages at the receiver's inputs to be rejected. The receiver then amplifies

only the differential input voltage within a very narrow frequency band and rejects all other input. Together, these mechanisms reject interference from external fields and enable very high CMTI and robust operation in the harsh electrical environments common in industrial applications.
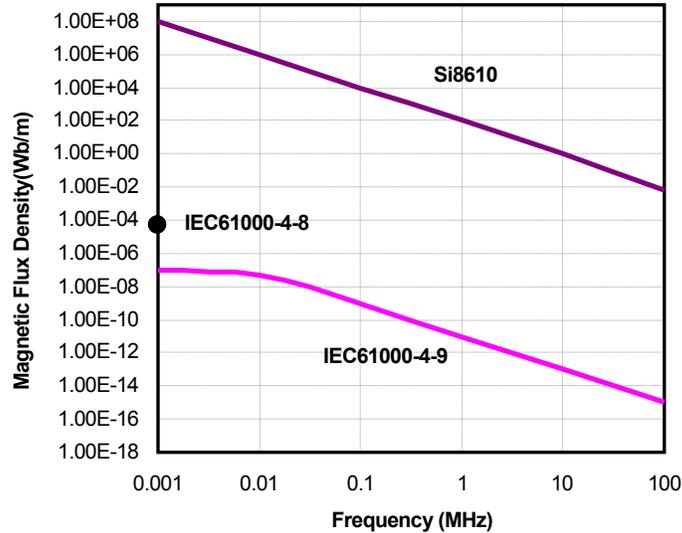


**Figure 12. CMOS Digital Isolator Magnetic Field Immunity**

As shown in Figure 12, the CMOS digital isolator's magnetic field immunity enables it to be used in close proximity to large motors and other magnetic field-producing equipment. It is theoretically possible that data transmission errors may occur if the magnetic field is too large and/or too close to the isolator. However, in actual use, the CMOS digital isolator provides extremely high immunity to external magnetic fields and has been independently evaluated to withstand magnetic fields of at least 1000 A/meter (per IEC 61000-4-8 and IEC 61000-4-9 specifications). A field of this kind can be generated by $10^7$ amperes through a 0.1 m conductor located 0.1 m away from the CMOS digital isolator. It is highly unlikely that such a condition would be found in any operating environment. Such a field would most likely destroy surrounding circuitry before damaging the isolation barrier of the CMOS isolator. In addition, the CMOS digital isolator has high electric field immunity (20 V/meter minimum) as measured by independent laboratories.

**Electrostatic Discharge (ESD) and Electrical Overstress (EOS)**

ESD and EOS events, such as fast transients and surges, can arise from any number of causes including ac line excursions, common-mode transients between grounds, lightning strikes, and human handling. ESD is a subset of these stresses, and testing at the IC package level provides a measurement of device robustness related to component handling (see Table 4).

**Table 4. CMOS Isolator ESD Test Summary**

|  | CMOS Digital Isolator | Optocoupler |
|---|---|---|
| **ESD TEST METHOD** | **PASS (V)** | **PASS (V)** |
| Human Body Model | ±6,000 | ±3,000 |
| Charge Device Model | ±2,000 | ±1,000 |
| Machine Model | 400 | Not Given |

While the CMOS digital isolator has higher ESD immunity than most optocouplers, it is important to note that testing consists of applying ESD directly to unpowered isolator pins. However, once installed

in a board, the isolator becomes part of a larger circuit where handling-related ESD hits are often diffused across lower impedance circuit paths. As a result, an isolator with a 6 kV ESD rating can reliably operate within a system having an ESD event of 15 kV. Protection against other EOS stresses must be addressed at the system level. Such considerations include proper layout techniques for minimizing noise, careful attention to short trace paths to minimize series inductance (and thereby circuit ringing), proper bias supply grounding, routing, and filtering, and protection against voltage and current surges.

**Application Examples**

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, the CMOS digital isolator needs only two external VDD bypass capacitors (0.22 to 1 µF) to operate. Its TTL level-compatible input terminals draw only micro amps of leakage current, allowing them to be driven without external buffering circuits. The output terminals have a characteristic impedance of 50 $\Omega$ (rail-to-rail swing) and are available in both forward and reverse channel configurations. Note that the circuit of Figure 13 is typical for most applications and is as easy to use as a standard CMOS logic gate.
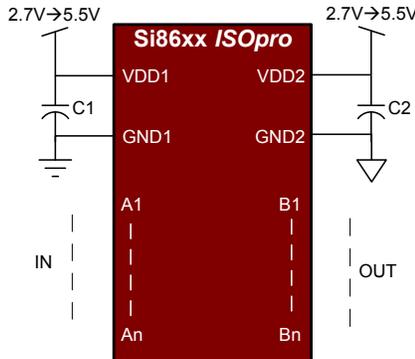


**Figure 13. CMOS Digital Isolator Application Schematic**

Figures 14, 15, and 16 show three different circuits recommended by optocoupler suppliers, each requiring additional external components when compared to the CMOS digital isolator. Figure 14 shows an isolated CMOS logic application. Here, a CMOS input buffer provides the correct input logic levels while supplying drive current for the optocoupler LED. Resistor $R_L$ limits LED current, and peaking capacitor Cp accelerates LED turn-on and turn-off time to reduce propagation delay to roughly 300 ns. The output circuit consists of a CMOS Schmitt trigger, which improves rise and fall time and provides additional noise immunity and low output impedance.
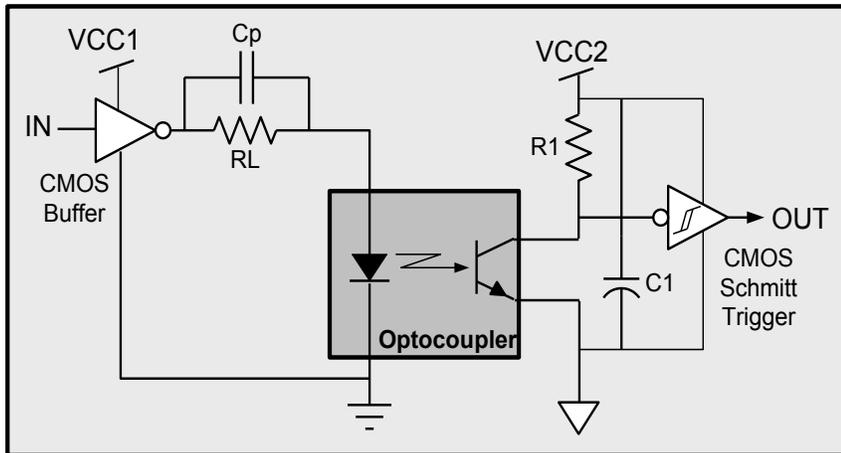


**Figure 14.  CMOS Driver**
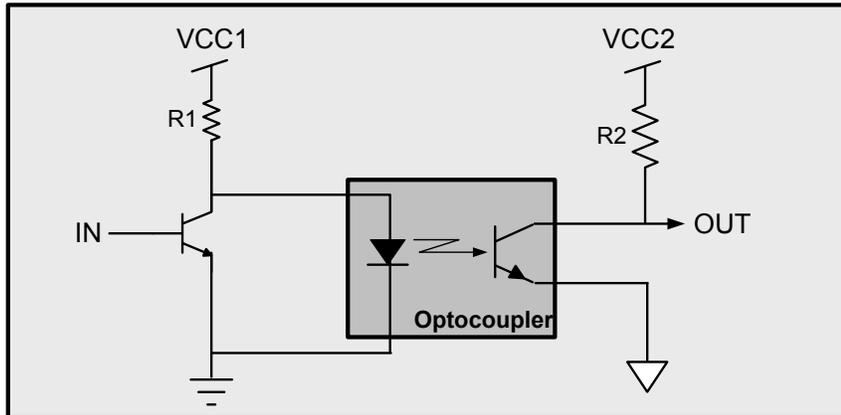
**Figure 15. High CMTI Isolator**
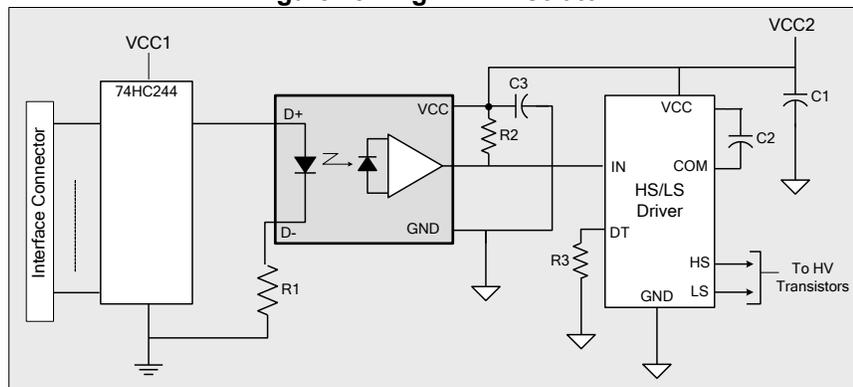


**Figure 16. Plasma Display Driver**

The circuit of Figure 15 trades higher power consumption and reduced LED life for improved CMTI. Note that this circuit can be combined with that of Figure 14 to improve its CMTI as well, but it requires additional external components. Resistor R1 has a relatively low value and overdrives the LED for improved CMTI when Q1 is off. The LED is turned off when transistor Q1 is on, shunting current around the LED to ground. Note that the efficiency of this circuit is poor because roughly the same amount of current is drawn from VCC1 whether the LED is off or on.

Figure 16 shows a high-voltage drive circuit for a plasma display. The incoming digital signal is conditioned by a logic buffer, which also provides drive current for the optocoupler LED. The optocoupler output drives a 600 V high-side/low-side driver, which, in turn, drives the high-voltage transistors that control the display.

Figures 17, 18, and 19 show the impact of the CMOS digital isolator on the circuits of Figures 14 through 16. In all cases, the CMOS digital isolator offers a substantial reduction in size and BOM while delivering better timing performance, lower power consumption, and higher reliability than the optocoupler. The circuits in Figures 17 and 18 show the CMOS digital isolator as a single-chip solution for the circuits shown in Figures 14 and 15. Figure 19 implements the circuit of Figure 16 using an ISOdriver, a device that combines RF isolation technology with a fully-featured, high-side/low-side IGBT/MOSFET driver capable of delivering up to 4 A peak.
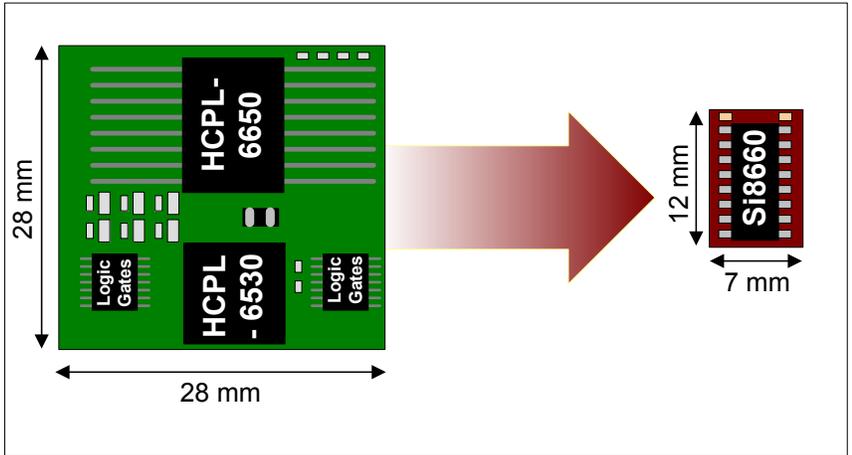
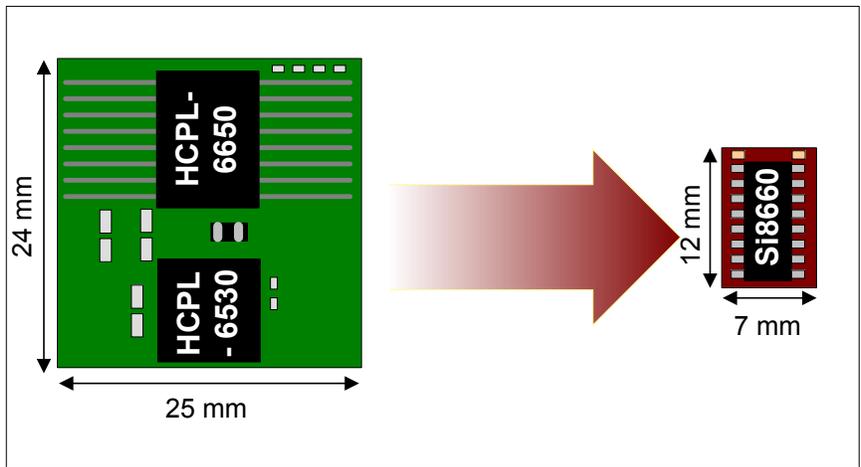**Figure 17.  6-Channel CMOS Isolator Level Shifter**
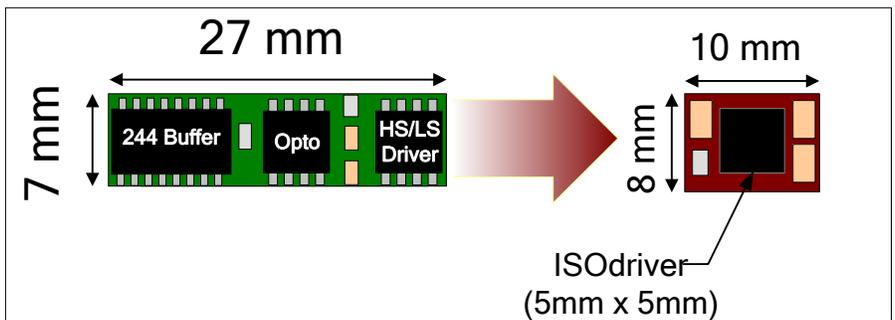


**Figure 18.  6-Channel High CMTI Isolator**



**Figure 19.  Single-Channel Plasma Display HV Driver**

Figure 20 shows an optocoupler supplier-recommended Profibus application implemented with three optocouplers and a differential bus transceiver, 75ALS176D. Profibus is an industrial serial communication standard that uses a twisted pair serial link. It is similar to RS-485 or 422 and can operate in either a low-speed (1.5 Mbps) or high-speed (12 Mbps) mode. Figure 21 shows a board-level implementation and the same circuit using the CMOS isolator approach.
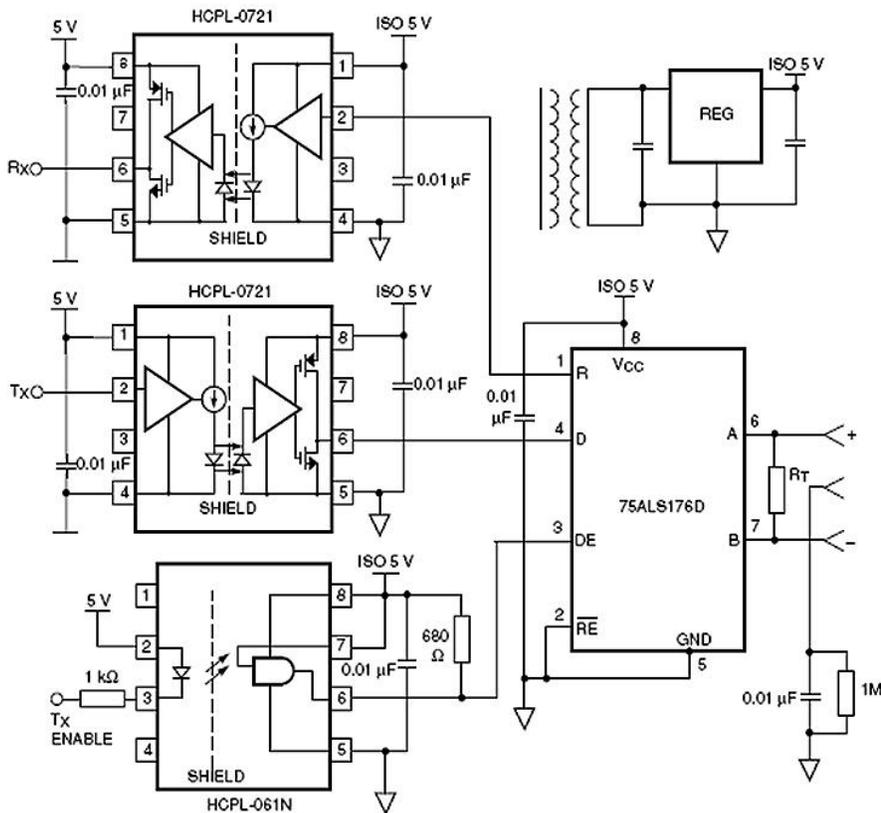


**Figure 20.  Isolated Profibus Transceiver**

In addition to saving over 100 square millimeters of space, the CMOS isolator implementation of Figure 21 provides four times faster propagation delay, three times better pulse width distortion, two times faster rise

and fall times, and three times better CMTI while consuming less than half the power of the optocoupler. Moreover, the CMOS digital isolator does not suffer from LOP or other wear-out mechanisms.
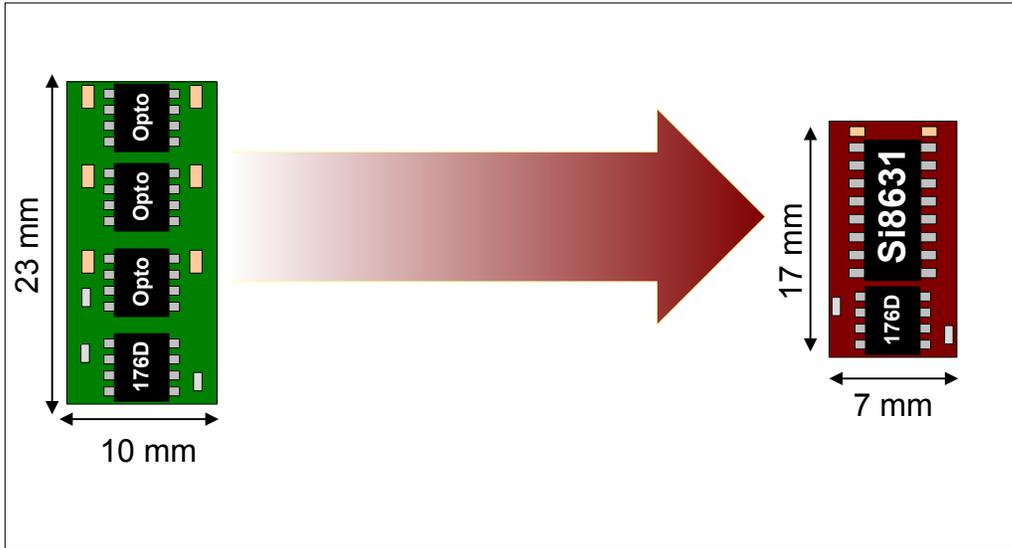


**Figure 21. Profibus Optocoupler Implementation vs. CMOS Digital Isolator**

The CMOS digital isolator external component savings for the above applications are summarized in Table 4. Clearly, the CMOS digital isolator's integration saves board space and cost, increases system reliability, and simplifies design. Table 4 summarizes the BOM savings for the CMOS isolator versions of Figures 13 and 15.

**Table 4. CMOS Isolator Circuit Implementations vs. Optocouplers**

| Circuit | Optocoupler Solution | | | CMOS Isolator Solution |
|---|---|---|---|---|
| | **Discrete Components** | **ICs** | **Total Opto BOM** | **Total BOM** |
| 6-Channel CMOS Interface | 19 | 4 | 23 | **3** |
| 6-Channel High CMTI | 13 | 2 | 15 | **3** |
| Plasma TV HV Driver | 4 | 3 | 7 | **3** |
| Profibus Communication Transceiver | 9 | 4 | 13 | **6** |

**Summary**

While optocouplers have been the dominant signal isolation device for many years, the advent of the RF isolator gives designers a smaller, more integrated, faster, and lower power alternative with none of the stability or wear-out mechanisms of optocouplers. The CMOS digital isolator is the best-in-class of all RF isolators and enables designers to access world-class isolator technology in a single package that is as easy to apply as a CMOS logic gate. Benefits of the CMOS digital isolator include:

- Higher integration: smaller size and lower cost-per-channel on multi-channel versions

- Higher performance: faster, tighter timing and substantially lower power

- Longer service life: no wear-out mechanisms as in optocouplers

- Higher reliability: operating parameters remain stable over VDD, temperature, and device age

- High CMTI: fully differential isolation signal path and high receiver selectivity for CMTI greater than 60 kV/µs

- Low EMI: meets FCC Class B Part 15

- High electric-field immunity: > 20 V/m, as measured by independent laboratories

- Industry-leading ESD tolerance: 6 kV HBM on all devices

- Lower external bill-of-materials: requires only two inexpensive VDD bypass capacitors

- Easy to use: single-chip, complete isolation solution

The history of the semiconductor industry is one of ever-increasing device performance and cost effectiveness with each process generation. Monolithic devices have always supplanted their hybrid counterparts, and RF isolation versus the hybridized optocoupler is no different. CMOS digital isolators *will* supersede optocouplers in industrial and many other applications. The trend has already begun.

**References**

1. Avago Optoisolation Selector Catalog, Avago Technologies
2. Avago Opto Designers Guide, Avago Technologies
3. EMI Test report for Si86xx Isolator Family, Silicon Labs 2016
4. Toshiba Opto Catalog BCE0034
5. Photo Relay white paper, Roger Shih, Toshiba America Electronic Components, Inc.