# A multi-mode, forced-frequency-resonant, high-performance flyback controller IC

## The XDPS21071

## Abstract

This is an introduction to Infineon's ZVS flyback controller which is suitable for USB PD applications, such as quick charger for mobile devices. This whitepaper discusses key features, as well as protection, operation, and control principles.

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# 1 Introduction

Recently, the demand for high-efficiency, high-density AC/DC charger and adapters is very common. This means that high-frequency designs can reduce the size of magnetic and other passive components. For high-frequency operation, zero-voltage switching is more conducive to reducing the turn-on loss of active switching components. Various zero-voltage switching (ZVS) topologies have been studied and corresponding controllers have been developed.

The discontinuous conduction mode (DCM) design can be selected for the USB PD application enabling ease-of-design and more stable control loop. The XDPS21071 [1] is a multi-mode controller with a built-in high-voltage start-up unit that can operate in DCM where using the adaptive CS compensation USB PD can improve system reliability. The start-up unit makes the IC power supply much more efficient and flexible during no-load operation. The nano DSP in the controller is like the brain of the chip. It makes the controller much "smarter" than traditional hardware mixed-signal devices. The digital and analog peripherals of XPDS21071 support a variety of signals sampling and conditioning, making it ideal for flyback operation. It integrates ZVS, frequency-reduction (FRM), and burst mode (BM) to obtain the best efficiency throughout the entire line and load regulation. In addition, a one-time-programming (OTP) memory is integrated to provide a variety of programmable parameters to simplify the design-in phase. Unlike mixed-signal peers, which require a large number of external resistor/capacitor networks to adjust parameters, digitally configurable pins simplify the system's BOM/PCB layout.

## 2 Quasi-resonant flyback issues

Equation 1 is the switching loss of quasi-resonant (QR) flyback switches at the first valley. $C_{para}$ includes both the MOSFET output capacitor and the transformer coupling capacitor. Therefore, on the low voltage line, QR flyback is almost a zero-voltage switch. But at the high line, there is still a lot of switching loss.

$$Psw(QR) = 0.5 * C_{para} * \left(V_{bus} - N_{ps} * V_{out}\right)^2 * f_{sw} \hspace{3cm} \textbf{Equation 1}$$

Another topology-related loss is the clamping network loss of the main MOSFET, and calculating that exact amount of loss is tricky.

After the main MOSFET is turned off, the primary peak current will first charge the parasitic capacitor of the main MOSFET and then transfer energy dump to the snubber network. Therefore, the larger the capacitor, the more energy stored in the parasitic capacitor, and the less wasted in the snubber. For hard switching, the loss in the parasitic capacitor disappears completely. But for QR flyback, some energy can be recycled. For full ZVS, most of the energy can be recycled even in high-voltage lines.

Therefore, the energy injected into the snubber network is ($0.5*L_{lk}*ipk^2-0.5*C_{para}*V_{sw}^2$). However, this is not all lost, and the actual loss depends on the snubber diode used. As shown in Figure 1, using a slow reverse-recovery diode can push a portion of the energy back to the bulk capacitor or output. The snubber network works only when $V_{sw}$-$V_{clamp}$-$V_{bus}$>0. This means that the snubber loss will be higher at low lines and lower at the high lines. Higher $C_{oss}$ absorbs more leakage energy, and using a ZVS controller means more leakage energy can be recovered. In addition, low $R_{DS(on)}$ MOSFETs can be used to reduce conduction losses and also reduce leakage losses.

Another problem is that the QR flyback operates at the lowest frequency under heavy load, which is not good for peak power applications in terms of transformer utilization.

The change of frequency change of the QR control frequency also can easily cause common-mode noise interference of the touch screen.

To simplify transformer manufacturing, PCB-based winding designs are preferred. To reduce copper losses, frequencies above 100 kHz are required. Also due to the large coupling capacitor of the PCB windings, the switching losses will be greater. Therefore, a fixed-frequency ZVS controller is required.
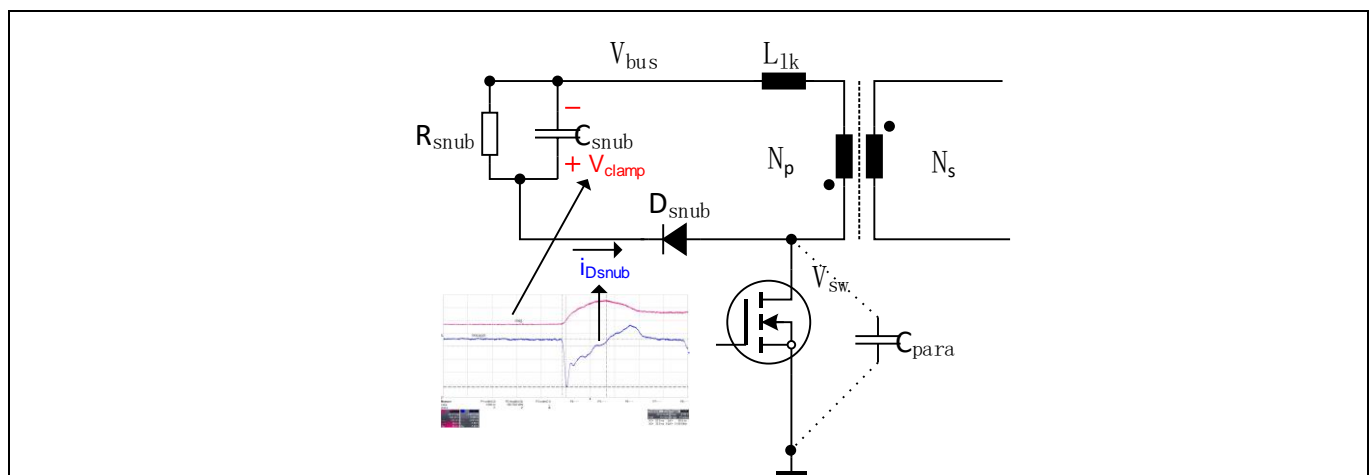


**Figure 1        Snubber waveforms**

# 3  Forced-frequency resonance zero-voltage-switching（FFRZVS）principles

Figure 2 shows a typical FFRZVS flyback PWM sequence and the associated key waveforms.

At $t_4$, after the main MOSFET is turned off, the MOSFET used for synchronous rectification (SR) will be delayed on for a short blanking time. At $t_5$, when the demagnetization current is ideally zero, the SR MOSFET is turned off, and then the magnetizing inductance ($L_p$) and the MOSFET-junction-equivalent capacitor ($C_{eqv}$) oscillate. The voltage of the main MOSFET will oscillate from $V_{bulk}+V_{refl}$ to $V_{bulk}-V_{refl}$, $V_{refl}=N_{ps}*V_o$. If the auxiliary MOSFET is turned on at $t_1$, the resonant peak of the main MOSFET, which means the magnetizing current is zero, and i_mag will be established in the negative direction. During this controlled ZVS on-time, the $V_{DS}$ of the main MOSFET is clamped to $V_{bulk}+V_{refl}$. Once the peak current reaches i_zvs_pk, the auxiliary MOSFET is turned off because this current is stored in the magnetizing inductance in reverse direction, so it will continue to flow in that direction and release energy stored in $C_{eqv}$. This duration in the IC is controlled by a configurable $t_{ZVSdead}$ parameter. Therefore, at $t_3$, the drain voltage of the main MOSFET reaches its minimum value, and then the main MOSFET can now be turned on with the lowest possible turn-on loss. As can be seen in the figure, the energy is proportional to $V_{bulk}$, and the ZVS on-time is also proportional.

After the leading-edge blanking (LEB) time of the turned-on main MOSFET, the MFIO voltage is sampled. Based on this voltage, the IC will know the switching frequency of the next cycle, switching cycle $T_{sw}$. Since the ZVS on-time and ZVS dead-time are also known, the $T_{sw}$-$T_{zvson}$-$T_{zvsdead}$ point determines the turn-on point of the ZVS MOSFET.

Since ZVS is achieved by the magnetizing inductance, ZVS is only valid during DCM. Through the active control of the pulse GD1, only the necessary amount of ZVS energy required, thereby reducing the circulating ZVS energy.
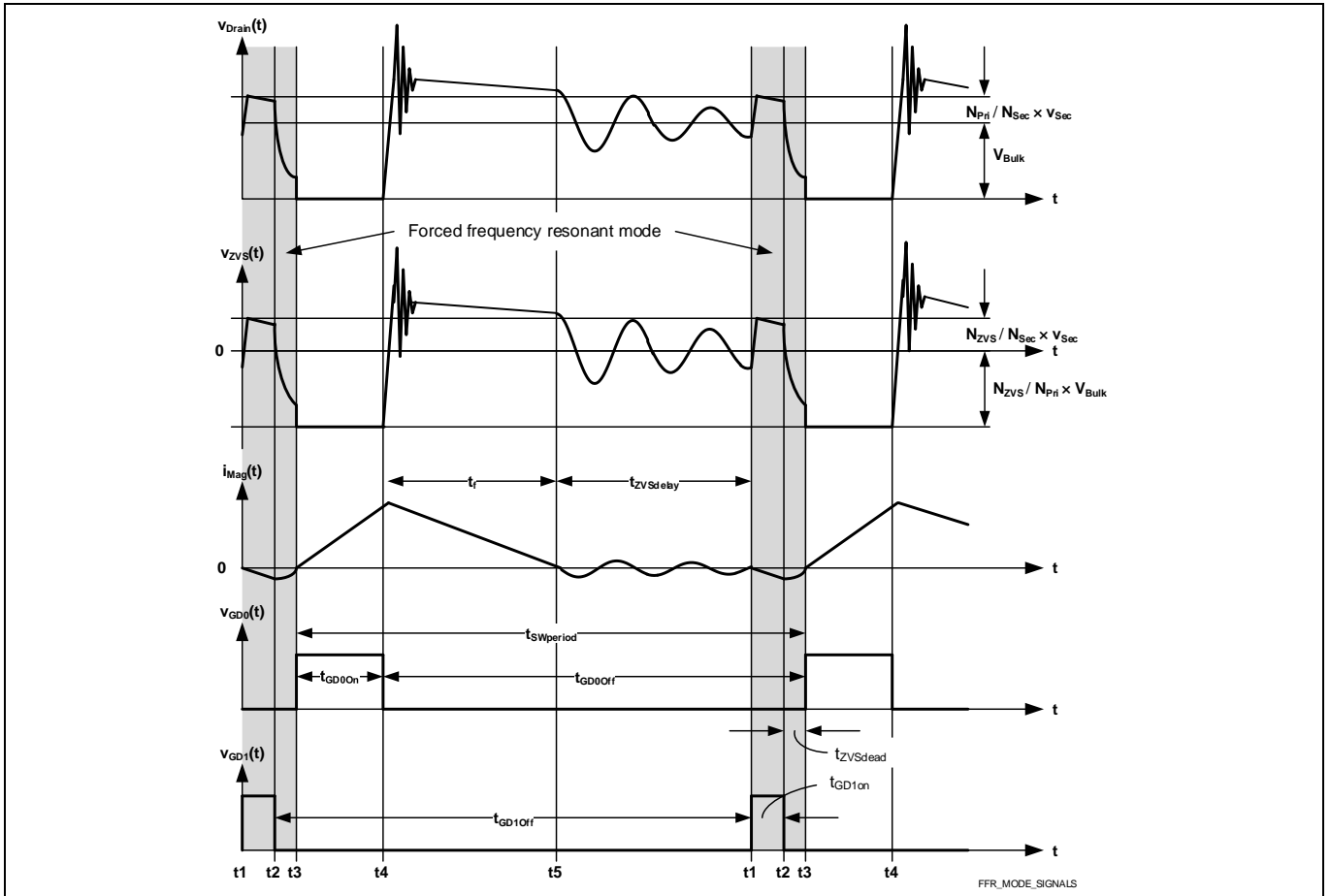
**Figure 2     ZVS principle visualization**

# 4 Simplified application diagram

Figure 3 shows the simplified application diagram for the flyback design using the XDPS21071. Compared with the conventional flyback, only one ZVS winding is added on the primary side, with a capacitor, switch and a low-side gate driver at the primary side. It does not require a high-side driver and a high-voltage MOSFET to achieve ZVS, so the system cost is lower.
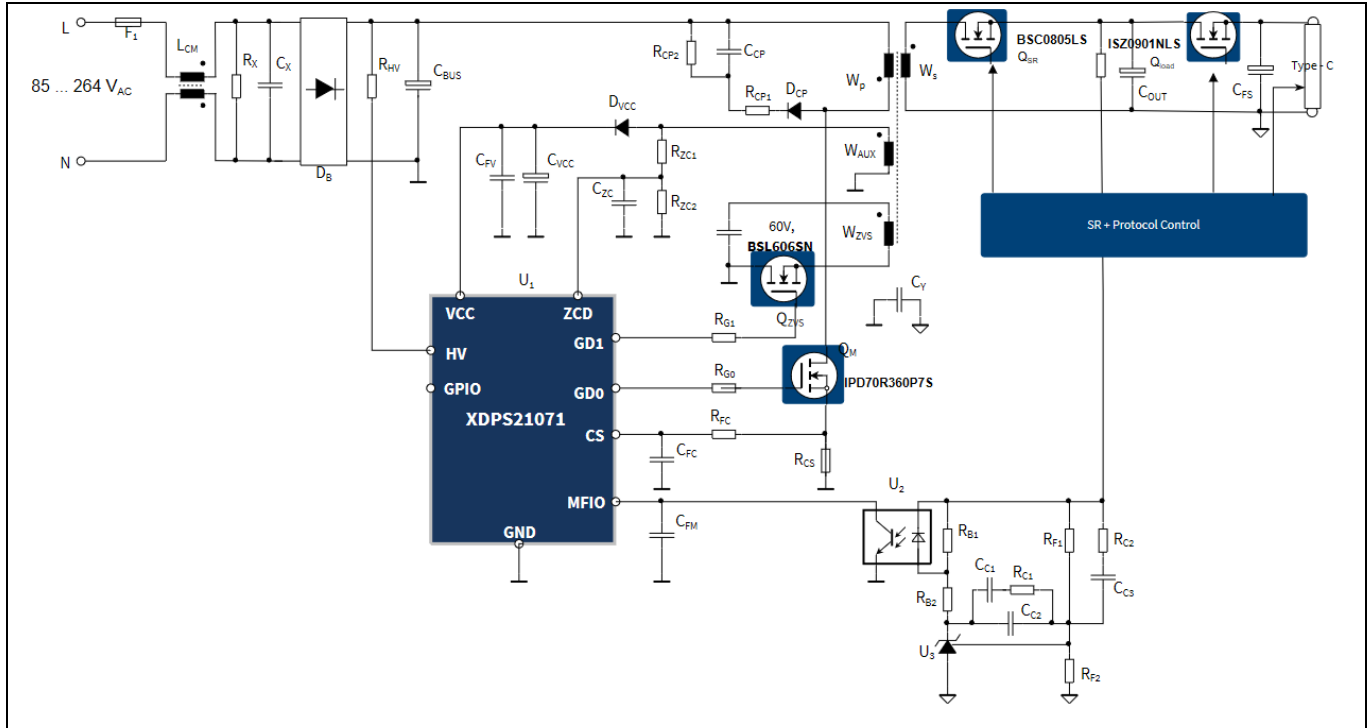


**Figure 3    Simplified application diagram of the XDPS21071 FFRZVS flyback controller IC**

# 5 A Working example – The 45 W USB PD quick charger reference design with the XDPS21071

Figure 4 shows a 45 W universal-input adapter reference design based on the XDPS21071 controller.
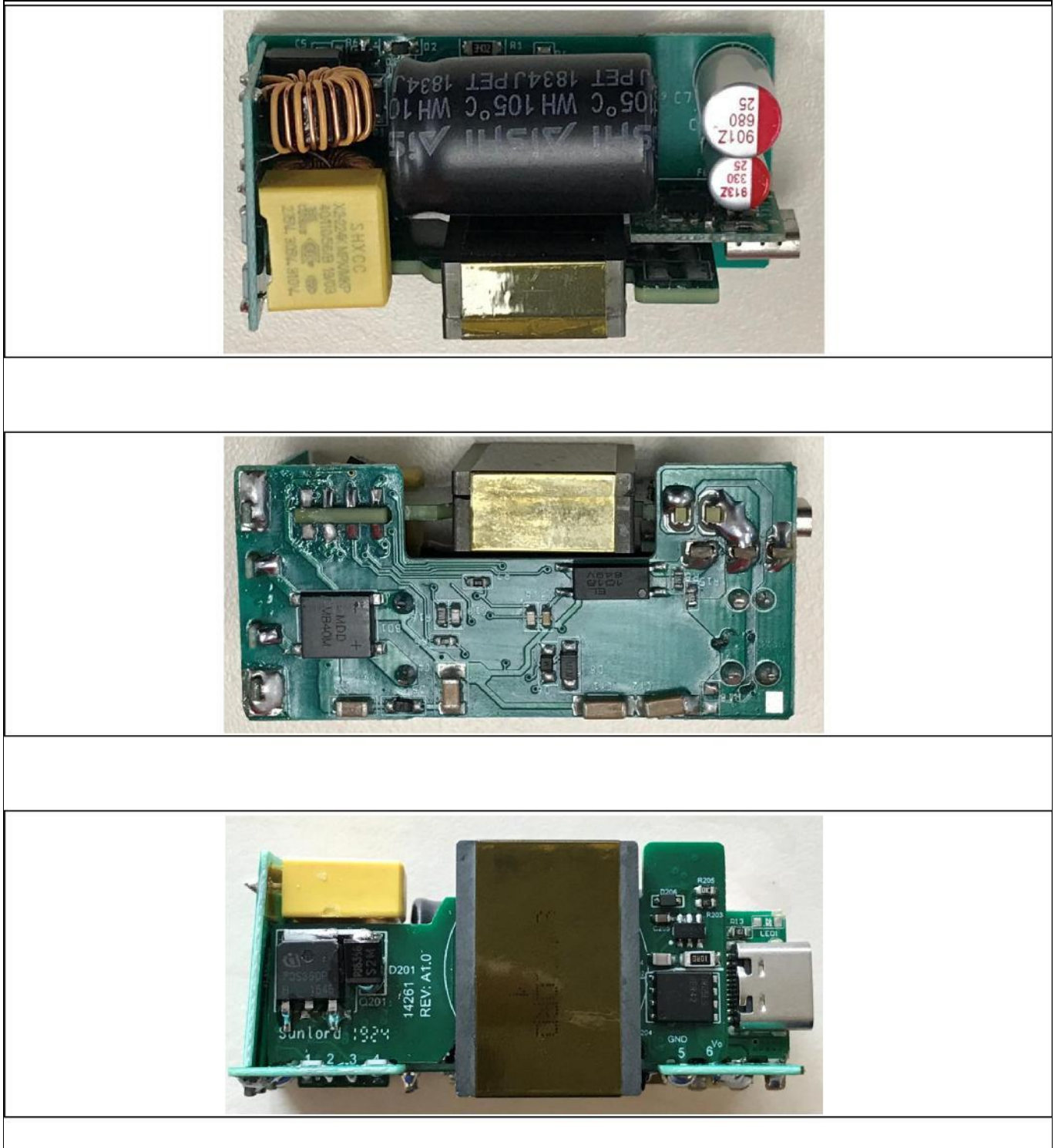


**Figure 4     The 45 W USB PD fast charger reference design from Infineon**

The FFRZVS controller XDPS21071 is operating in a guaranteed DCM mode under all conditions. XDPS21071 also implements FRM and BM to maximize efficiency at light and medium loads.

The technical specifications of the reference design are as follows:

› AC input voltage range: 90 – 264 V
› DC output voltage range: 5 – 20 V
› Switching frequency: 120 kHz
› Turns ratio ($N_p$:$N_s$): 7
› Transformer primary winding inductance ($L_p$): 210 µH
› Bulk capacitor: 82 µF
› Main MOSFET: IPD70R360P7S
› ZVS MOSFET: BSL606SN
› SR MOSFET: BSC0805LS

The use of a flat transformer can further increase power density and minimize system size. The best power density for this type of adapter is 15 W/in$^3$ (including casing). The inputs include a common-mode choke and a differential choke. The PCB board terminal-efficiency results are shown below. It meets the EC COCV5 Tier 2 and the DOELV6 standards.
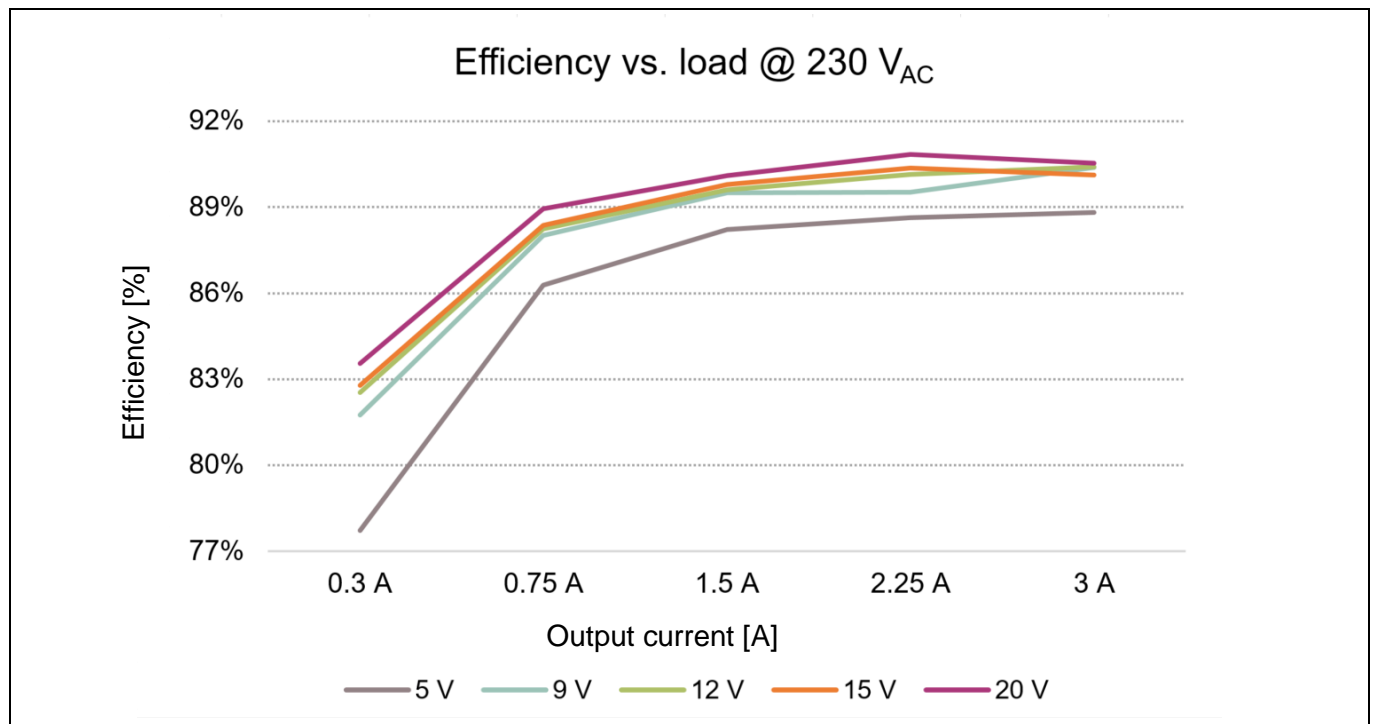


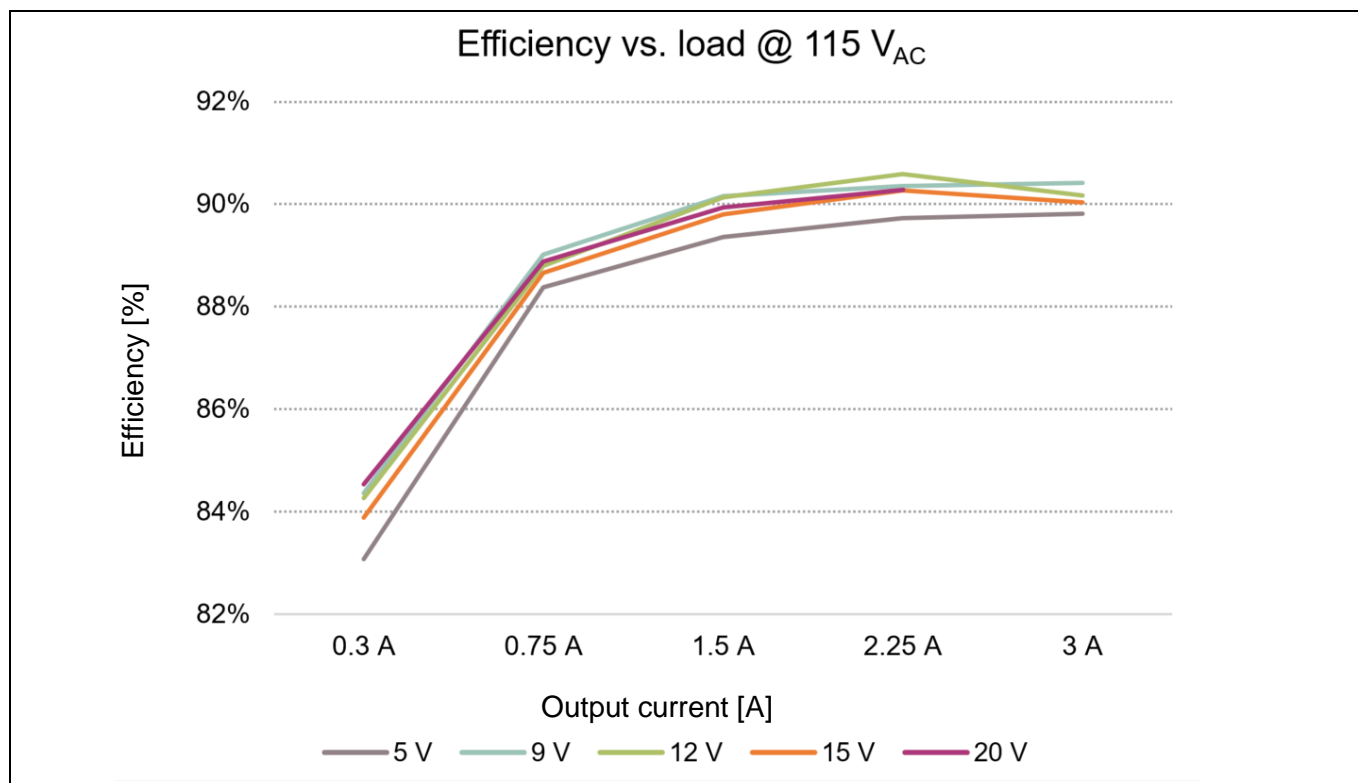**Figure 5    Efficiency under 230 $V_{AC}$**

**Figure 6    Efficiency under 115 V$_{AC}$**

## 5.1      Thermal measurement results

Thermal results were checked after three hours of burn-in in an open frame at room temperature at different input voltages of 20 V/2.25 A. SR IC was covered by a thermal pad. A thermal coupler was used to measure the temperature of different components.

**Table 1          Thermal results**

|  | 90 V$_{AC}$ | 115 V$_{AC}$ | 230 V$_{AC}$ | 264 V$_{AC}$ |
|---|---|---|---|---|
| SR MOSFET | 91.0°C | 92.3°C | 97.4°C | 98.0°C |
| Primary MOSFET | 97.0°C | 98.3°C | 92.7°C | 93.6°C |
| Transformer core | 88.0°C | 88.8°C | 96.6°C | 99.0°C |
| Transformer copper | 83.0°C | 83.8°C | 86.2°C | 87.0°C |
| Input rectifier | 83.6°C | 77.4°C | 68.6°C | 67.8°C |
| XDPS21071 | 71.2°C | 71.0°C | 72.4°C | 72.8°C |
| SR IC | 77.1°C | 78.1°C | 84.2°C | 85.3°C |
| Primary MOSFET snubber diode | 84.8°C | 87.0°C | 84.0°C | 84.0°C |
| Secondary MOSFET snubber | 76.0°C | 77.3°C | 83.6°C | 85.0°C |

## 5.2 Operating waveforms of the 45 W quick charger design

The system design specifications are 90 - 264 $V_{AC}$ input, 5 - 20 V output, and peak power 20V/2.25 A. The main MOSFET used is the IPD70R360P7S, the SR MOSFET is the BSC0805LS. A customized planar transformer is used. The power density that can be achieved is 20.6 W/in$^3$ (with PCBA). Table 2 shows the drain waveforms.

The ZVS switch is implemented by ZVS winding, which has a low-voltage MOSFET Q2 BSL606N. During DCM, the ZVS MOSFET Q2 turns on for a short time (the turn-on time depends on input voltage) before the main MOSFET Q1 is turned on, so the drain-source voltage of the main MOSFET would drop to a lower voltage before it turns on to achieve ZVS switching. Ch1 is the $V_{DS}$ of the primary main MOSFET with a peak voltage of 558 V, Ch2 is the $V_{DS}$ of the secondary SR MOSFET with a peak voltage of 77.8 V.
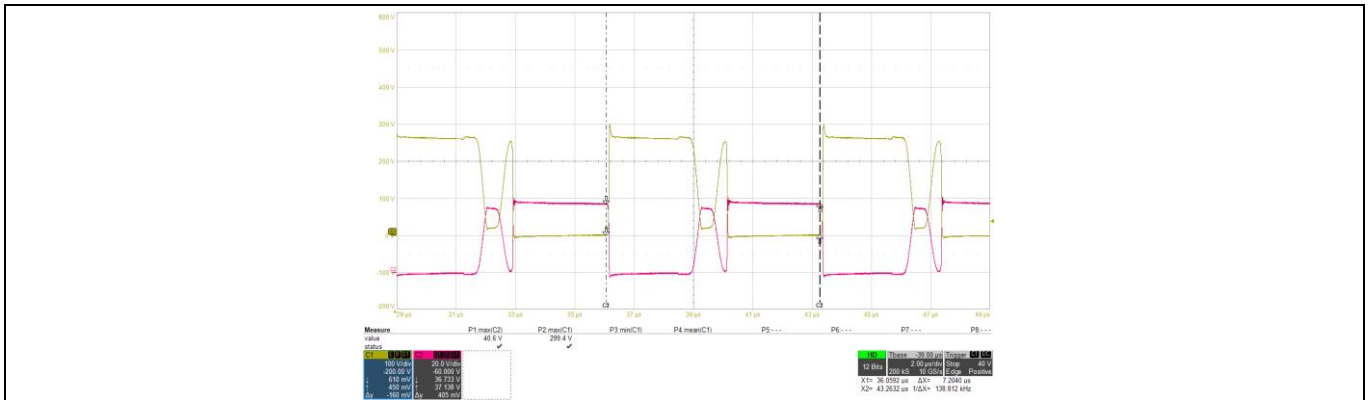


**Figure 7** **Drain waveforms of the primary-side MOSFET under different line/output**
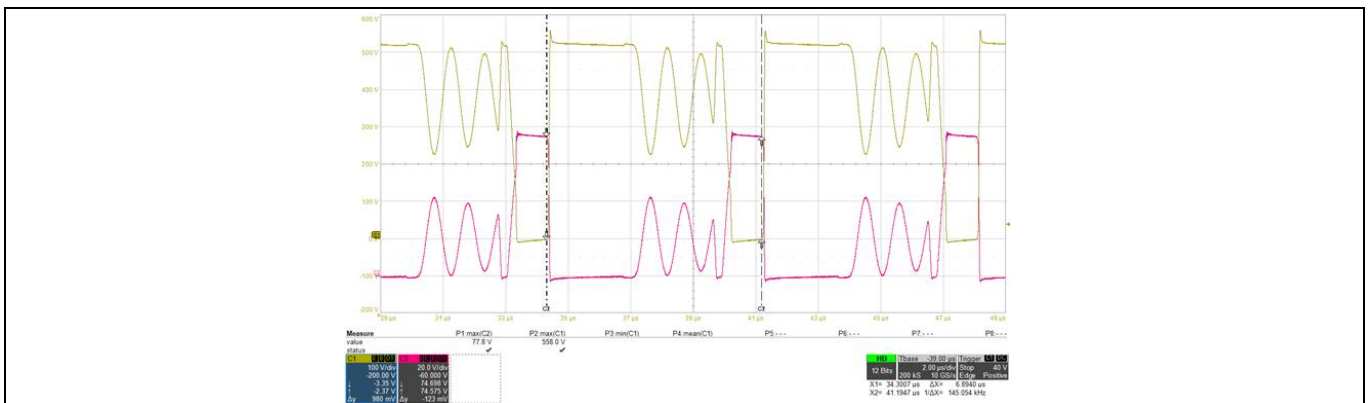Ch1 $V_{DS\_Pri\ MOS}$, Ch2 $V_{DS\_SR}$, switching waveform at $V_{AC}$ = 90 V and 20 V/2.25 A



**Figure 8** **Drain waveforms of primary-side MOSFET under different line/output**
Ch1 $V_{DS\_Pri\ MOS}$, Ch2 $V_{DS\_SR}$, ZVS switching waveform at $V_{AC}$ = 264 V and 20 V/2.25 A

## 5.3 Conducted emissions (EN 55022 class B)

Conducted EMI is measured by a certified safety laboratory in accordance with the EN 55022 (CISPR 22) class B test standards. The demonstration board was set up at a different output full load at input voltages

of 110 V$_{AC}$ and 230 V$_{AC}$. The system passed the CISPR 22 class B standard testing. Because it is close to the input pins, a copper heatsink was used to cover the main MOSFET to improve the EMI testing.

**Table 2      EMI test results under different output full loads**

| Output voltage (V) | 120 V/L | 120 V/N | 230 V/L | 230 V/N |
|---|---|---|---|---|
| 5 | Pass | Pass | Pass | Pass |
| 9 | Pass | Pass | Pass | Pass |
| 12 | Pass | Pass | Pass | Pass |
| 15 | Pass | Pass | Pass | Pass |
| 20 | Pass | Pass | Pass | Pass |



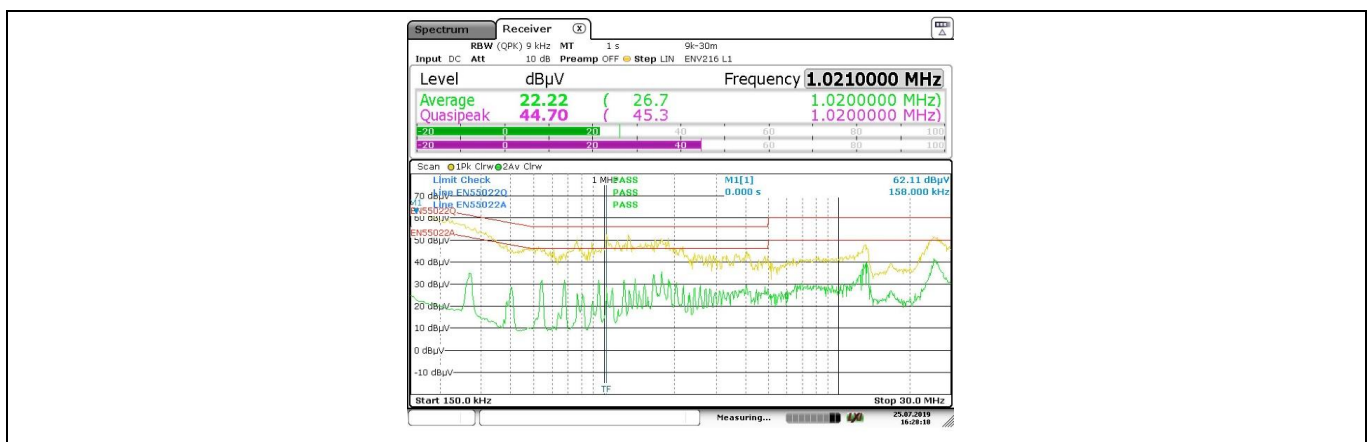**Figure 9    Conducted EMC**
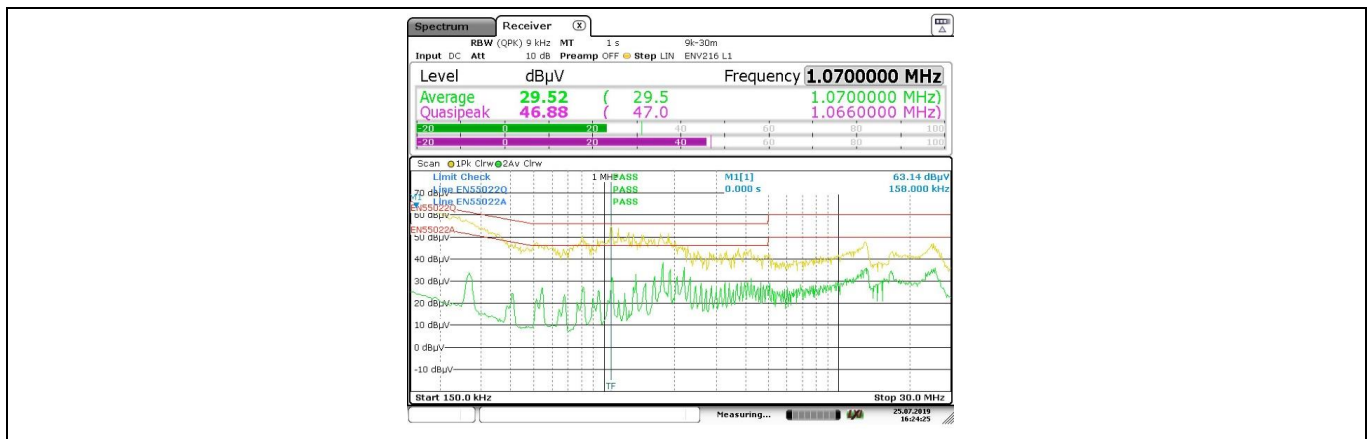120 V$_{AC}$, 20 V/2.25 A - Neutral



**Figure 10  Conducted EMC**
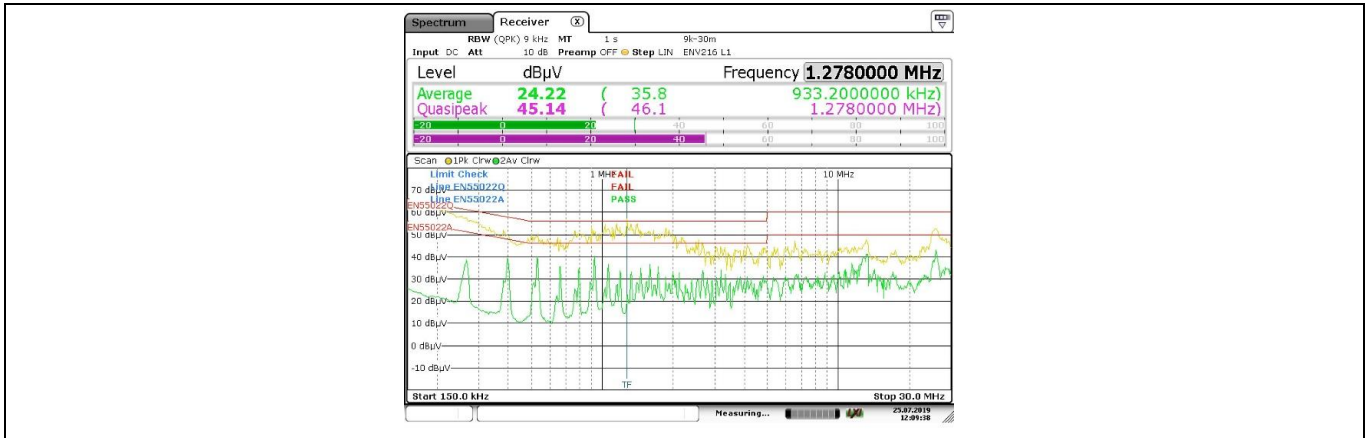120 V$_{AC}$, 20 V/ 2.25 A - Line

**Figure 11  Conducted EMC**
230 V$_{AC}$, 20 V/2.25 A - Neutral
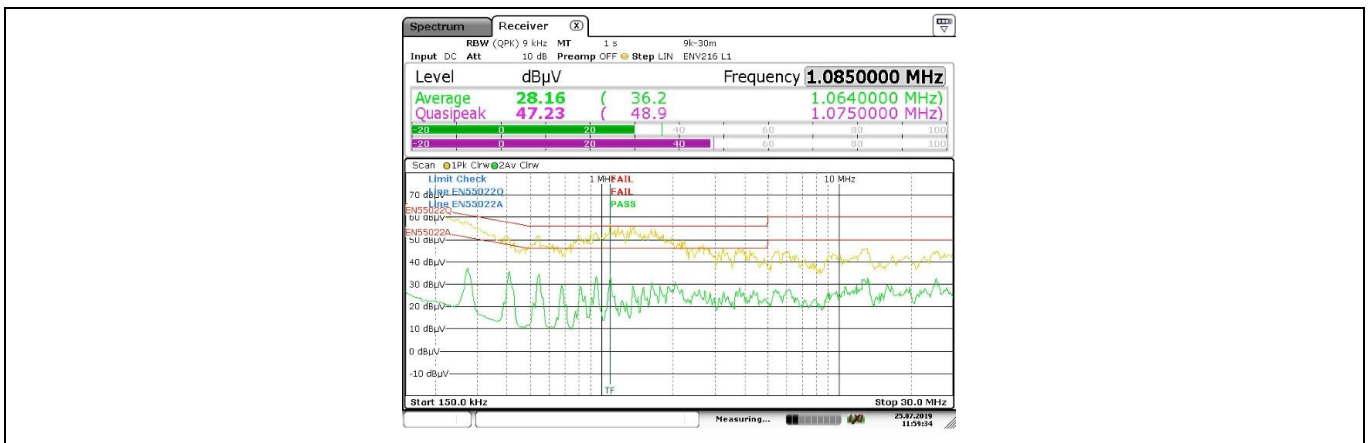


**Figure 12  Conducted EMC**
230 V$_{AC}$, 20 V/2.25 A - Line

## 5.4      Standby and light load operation

Low standby power consumption is a key feature of a charger design. The 45 W reference design fully meets the standby power requirements. Standby power consumption is measured from 90 V$_{AC}$ to 264 V$_{AC}$ at the default 5 V output, and it is less than 30 mW in all cases. Standby power was measured for one minute with a WT210 Yokogawa power meter.

Table 3 shows the standby power consumption according to various inputs.

**Table 3         Standby power consumption**

| V$_{out}$ [V] | Load [A] | AC input voltage [V] | Input power [mW] |
|---|---|---|---|
| 5 | 0 | 90 | 19 |
| | | 115 | 19.6 |
| | | 230 | 20 |
| | | 264 | 22 |

BM is important for primary AC/DC controllers to meet no-load requirements. Generally, when the feedback is below a certain value, the IC will enter BM. To reduce output voltage ripple, BM operation hysteresis needs to be as small as possible. This is a considerable challenge for variable output voltage designs. However, due to digital control, the XDPS21071 implements BM entry based on a lookup table, and it will change the BM entry conditions based on different output voltages.

Table 4 shows the current that enter and leave the line in BM. Stable and consistent results are achieved.

**Table 4        Burst mode entry/exit output current under different line/$V_o$**

| $V_o$ [V] | 5 | | 9 | | 12 | | 15 | | 20 | |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IN(AC)}$ | $I_{o\_ent}$ [A] | $I_{o\_lea}$ [A] | $I_{o\_ent}$ [A] | $I_{o\_lea}$ [A] | $I_{o\_ent}$ [A] | $I_{o\_lea}$ [A] | $I_{o\_ent}$ [A] | $I_{o\_lea}$ [A] | $I_{o\_ent}$ [A] | $I_{o\_lea}$ [A] |
| 90 | 0.185 | 0.388 | 0.096 | 0.196 | 0.097 | 0.148 | 0.048 | 0.112 | 0.038 | 0.103 |
| 115 | 0.179 | 0.388 | 0.091 | 0.212 | 0.109 | 0.170 | 0.051 | 0.113 | 0.044 | 0.081 |
| 230 | 0.218 | 0.455 | 0.097 | 0.238 | 0.110 | 0.170 | 0.030 | 0.112 | 0.027 | 0.094 |
| 264 | 0.273 | 0.561 | 0.096 | 0.316 | 0.116 | 0.224 | 0.038 | 0.163 | 0.032 | 0.126 |

# 6 Configurable parameters using Heading4 GUI of dpVision®

The table in Figure 13 lists all the configurable parameters of the XDPS21071. All these parameters can be changed through the UART pins, which greatly simplifies the system BOM. Since many application-related parameters are adjustable, the controller can be tailored for different system designs. For example, the configurable frequency law can be used to adjust the maximum frequency to suit different magnetics-core shape, and adjust the middle load efficiency to balance conduction- and switching losses. Configurable BM parameters can be used to adjust BM entry and exit power.

| Hardware Configuration | | |
|---|---|---|
| **Control Feature** | | |
| k_PDC | 8400 | |
| k_PDC_OFFSET | 0 | |
| t_CSLEB | 269 | ns |
| t_ZVSdead | 300 | ns |
| k_ZVSon | 8000 | |
| I_GD0_Drive | 31 | mA |
| **Protection** | | |
| T_JOTP | 130 | degreeC |
| t_OCP2 | 600 | ns |
| t_PeakPower | 30 | ms |
| EN_PeakPower | Enabled | |
| Response_OVP | Auto-Restart | |
| **Burst Configuration** | | |
| Vcs_Burst | 0.128 | V |
| Freq_Burst | 50.0 | KHz |
| v_Burst_Pause | 1.35 | V |
| v_Burst_Exit | 2.00 | V |
| t_ReEntry_Burst | 5 | ms |
| t_Quiet_Burst | 0.1 | ms |
| **Frequency Law** | | |
| Freq_Law_Max | 120.0 | KHz |
| MFIO_Point_C | 1.00 | V |
| MFIO_Point_B | 1.80 | V |
| Vcs_at_Point_BC | 0.45 | V |
| Freq_cap_at_special_condition | 90.0 | KHz |
| **Adaptive Vcs offset** | | |
| k_Vcs_offset | 28000 | |
| Vcs_offset_Vzcdzeropoint | 148 | |
| EN_Vcs_offset | Enabled | |

**Figure 13   Configurable parameters of the XDPS21071**

# 7 Summary

The FFRZVS topology with optimized system design shows a good performance/cost implementation of a 45 W quick charger with superjunction high-voltage MOSFETs and OptiMOS™ power MOSFETs. The digital control of the XDPS21071 makes many parameters adjustable, therefore simplifies BOM. It also provides power-supply engineers with a great flexibility, allowing them to tailor-make their designs based on different system specifications. The 45 W reference design can be easily expanded to 65 W using a similar scheme.

## References

[1]    Datasheet of the XDPS21071

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