Silicon Labs Timing Reference Designs

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Partner Reference Designs

Silicon Labs

Timing Solutions for Broadcom Switches/PHYs

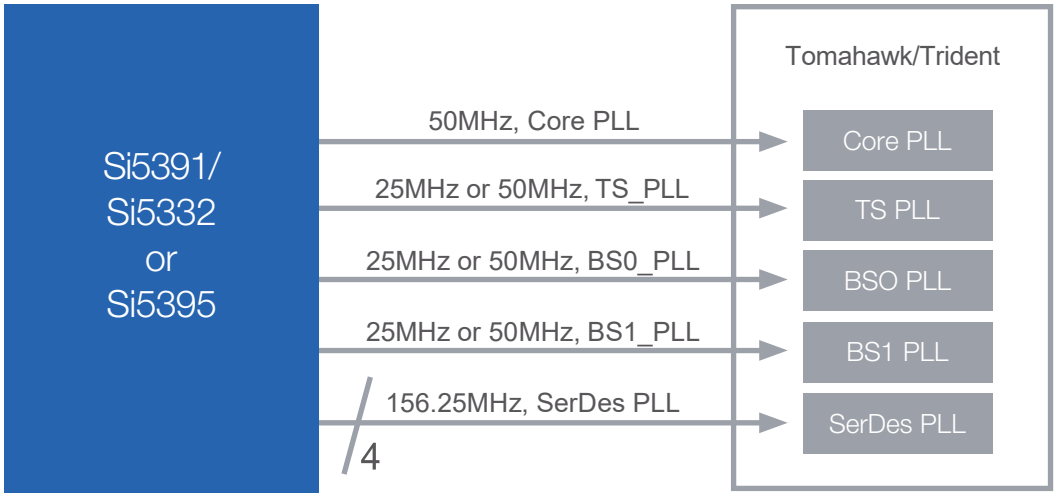
Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.

Timing Solutions for Tomahawk/Trident Switches



For more information related to reference designs or partner pricing, please contact your local Silicon Labs sales representative.

Oscillators

- Any frequency up to 3.0 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs
- PCI Express Gen 1/2/3/4/5 compliant

Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Timing Solutions for Broadcom

Application		Broadcom Product Family	Silicon Labs XO	Silicon Labs Clock Buffer	Silicon Labs Clock
Broadband	DSL/G.fast/Cable Central Office	BCM33xx BCM65xxx	Si51x Si53x/Si54x/Si57x	Si5330x	Si5332 Si5341
	xPON OLT	BCM68xxx BCM55xxx	Si51x Si53x/Si54x/Si57x	Si5330x	Si5332 Si5341
Enterprise + Network Processors	StrataGX Communications Processors	BCM58xxx XLPxxx	Si51x	Si5330x	Si5332
	Knowledge-Based Processors	NLxxx NLAxxx	Si51x	Si5330x	Si5332
Wireless Infrastructure	Small Cells	BCM616xx	Si51x	Si5330x	Si538x
	DFE Processors	BCM510xx	Si51x	Si5330x	Si538x
	Microwave / Mobile Backhaul	BCM85xxx	Si51x Si53x/Si54x/Si57x	Si5330x	Si534x Si538x
Ethernet Communication + Switching	10G/25G/50G StrataConnect Switch	BCM53570	Si54x	Si5330x	Si5332 Si5341
	10/40/100G Retimer/ Gearbox	BCM82xxx	Si53x/Si54x	Si5330x	Si534x
	10/100GbE PHY/retimer	BCM82xxx BCM81xxx	Si53x/Si54x	Si5330x	Si534x
	200/400 GbE PHY/Retimer	BCM81xxx	Si54x	Si5330x	Si539x
	10/40/100GbE Trident/ Tomahawk Switch	BCM56860 BCM56870/970	Si54x	Si5330x	Si5332
	200/400GbE Tomahawk Switch	BCM56980	Si54x	Si5330x	Si539x
Storage Adapters and Controllers	SAS/SATA/NVMe Host Bus Adapters	HBA 9xxx	Si51x	Si5315x/ Si5330x	Si5332
	Fibre Channel Host Bus Adapters	LPe3200x	Si51x	Si5315x/ Si5330x	Si5332
	SAS/SATA Storage Controllers	SAS2xxx SAS3xxx	Si51x	Si5315x/ Si5330x	Si5332
	Fibre Channel Storage Controllers	XE2xx XE5xx	Si51x	Si5315x/ Si5330x	Si5332

Broadcom Switch/PHY Jitter Requirements

Timing solutions from Silicon Labs meet Broadcom reference clock jitter requirements with significant margin.

Broadcom Family	Chipset	Frequency	Silicon Labs Device	BRCM Jitter Requirement	Silicon Labs RMS Jitter
Strata XGS	Trident2	4x 156.25MHz	Si5332 Clock Generator or Si5345 JA Clock	0.3ps	217fs RMS
		25 or 50MHz		2ps	209fs RMS
	Trident3	4x 156.25MHz		0.3ps	217fs RMS
		25 or 50MHz		2ps	209fs RMS
	Tomahawk1	4x 156.25MHz		0.3ps	217fs RMS
		25 or 50MHz		2ps	209fs RMS
	Tomahawk2	4x 156.25MHz	Si5341 Clock Generator or Si5345 JA Clock	0.15ps	83fs RMS
		25 or 50MHz		2ps	170fs RMS
	Tomahawk3	8 x 312.5MHz	Si5391P Clock Generator or Si5395P JA Clock	0.15ps	68fs RMS
		100MHz		0.2ps	120fs RMS
		25 or 50MHz		0.2ps	120fs RMS

For more information, visit **silabs.com/timing**

Request a custom clock or XO/VCXO at **silabs.com/custom-timing**

Silicon Labs

Silicon Labs Timing Solutions for Intel FPGAs

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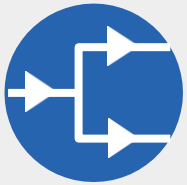

Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
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Recommended Timing Solutions vs Intel

*Yes, but without spread spectrum
Note 1: Jitter integration band defined by jitter tolerance mask (receiver CDR) and XCVR PLL multiplying BW (20MHz default)
Note 2: Jitter defined by standard or as budgeted fraction of transmitter eye closure

Industry Standard Interface		Jitter Band [1] (MHz)	Max Jitter[2] (fs rms)	Intel												Silicon Labs											
				Agilex			Stratix				Arria			Cyclone			XO/VCXO				Buffer		Clock Gen				Jitter Atten. Clock	
				F Series	I Series	M Series	10 TX	10 GX/SX	10 MX	V GX/GS	10 GT	10 GX/SX	10 GX	V GX/SX	V GT/ST	Si51x	Si59x	Si54x	Si56x	Si532xx	Si533xx	Si522xx	Si5332	Si5341	Si5391	Si534x/8x	Si539x
OIF	CEI-6G-SR/LR	4-20	630	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	CEI-11G-SR	8-20	380	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓		✓	✓	✓	✓	✓
	CEI-28G-VSR	16-20	150	✓	✓	✓	✓	✓	✓										✓	✓					✓	✓	✓	✓
	CEI-56G-PAM4-MR/LR	4-20	350	✓	✓	✓	✓												✓	✓		✓		✓	✓	✓	✓	✓
	CEI-56G-PAM4-VSR	4-20	240	✓	✓	✓	✓												✓	✓				✓	✓	✓	✓	✓
	CEI-112G-PAM4-VSR	4-20	120[(3)]		✓	✓													✓	✓						✓		✓
	SFI-5.1	4-20	1300	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	SFI-5.2	4-20	380	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
IEEE 802.3	1000BASE-X (GbE)	0.6-10	3000	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	10GBASE-R	0.6-20	430	✓	✓	✓	✓	✓	✓	✓			✓						✓	✓		✓		✓	✓	✓		✓
	10GBASE-KR	0.6-20	430	✓	✓	✓	✓	✓	✓	✓			✓						✓	✓		✓		✓	✓	✓	✓	✓
	400GAUI-8 C2C	4-20	380	✓	✓	✓	✓												✓	✓		✓		✓	✓	✓	✓	✓
	400GAUI-8 C2M	4-20	275	✓	✓	✓	✓												✓	✓		✓		✓	✓	✓	✓	✓
	CDAUI-16 (400GbE)	4-20	480	✓	✓	✓	✓	✓	✓								✓		✓	✓		✓		✓	✓	✓	✓	✓
	CDAUI-8 (400GbE)	4-20	240	✓	✓	✓	✓												✓	✓				✓	✓	✓	✓	✓
	CAUI-4	1.9-10	280	✓	✓	✓	✓	✓	✓		✓								✓	✓		✓		✓	✓	✓	✓	✓
	CAUI-10	1.9-4	460	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓		✓	✓		✓		✓	✓	✓	✓	✓
	XAUI 10GBASE-X	0.6-20	430	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓			✓	✓		✓		✓	✓	✓	✓	✓
	XLAUI (40GbE)	0.6-20	430	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓			✓	✓		✓		✓	✓	✓	✓	✓
	OTN (OTU/EPON)	0.6-20	430	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓			✓	✓		✓		✓	✓	✓	✓	✓
	SGMII/QSGMII	4-20	1400	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓

*Yes, but without spread spectrum
Note 1: Jitter integration band defined by jitter tolerance mask (receiver CDR) and XCVR PLL multiplying BW (20MHz default)
Note 2: Jitter defined by standard or as budgeted fraction of transmitter eye closure

				Intel												Silicon Labs											
				Agilex			Stratix				Arria		Cyclone			XO/VCXO				Buffer		Clock Gen				Jitter Atten. Clock	
Industry Standard Interface		Jitter Band [1] (MHz)	Max Jitter[2] (fs rms)	F Series	I Series	M Series	10 TX	10 GX/SX	10 MX	V GX/GS	10 GT	10 GX/SX	10 GX	V GX/SX	V GT/ST	Si51x	Si59x	Si54x	Si56x	Si532xx	Si533xx	Si522xx	Si5332	Si5341	Si5391	Si534x/8x	Si539x
Proprietary	RXAUI/DXAUI	1.9-20	950	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
ITU	GPON	0.6-10	1500	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
CPRI	CPRI 10G	various	Various 10G+	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓					✓	✓		✓		✓	✓	✓	✓	✓
	CPRI 12G	various	Various 12G+	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓					✓	✓		✓		✓	✓	✓	✓	✓
	CPRI 24G	various	Various 24G+	✓	✓	✓	✓	✓	✓		✓							✓	✓		✓			✓	✓	✓	✓
INCITS/T11	Fibre Ch – 8G, 16G	0.6-10	240	✓	✓	✓	✓	✓	✓	✓	✓	✓						✓	✓		✓		✓	✓	✓	✓	✓
	Fibre Ch – 32G	0.6-10	130	✓	✓	✓	✓	✓	✓		✓							✓	✓		✓			✓	✓	✓	✓
JEDEC	JESD204B	various	Per DAC/ADC	✓	✓	✓	✓	✓	✓	✓	✓	✓												✓	✓	✓	✓
Intel	Interlaken – 6G	4-20	630	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	Interlaken – 10G	4-20	380	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓		✓	✓		✓		✓	✓	✓	✓	✓
	QPI	Intel	200	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI-SIG	PCI Express Gen3	various	1000	✓	✓	✓	✓	✓	✓	✓	✓	✓				*	*	*	*	✓	✓	✓	✓	*	*	*	*
	PCI Express Gen4	various	500	✓	✓	✓										*	*	*	*	✓	✓	✓	✓	*	*	*	*
	PCI Express Gen5	various	150		✓	✓										*	*	*	*	✓	✓	✓	✓	*	*	*	*
CCIX	CCIX-25G	various	350	✓	✓	✓										*	*	*	*	✓	✓		✓	*	*	*	*
SATA-IO	SAS/SATA 6G	2.6-15	780	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	SAS/SATA 12G	2.6-15	390	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓		✓	✓		✓		✓	✓	✓	✓	✓
SMPTE	SDI 3G, 6G	0.1-F/2	800	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	SDI 12G	0.1-F/2	400	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓		✓	✓	✓	✓	✓
	SDI 24G	0.1-F/2	200[3]	✓	✓	✓	✓	✓	✓		✓							✓						✓	✓	✓	✓
RapidIO	RapidIO-1, -2, -3	4-20	410	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓		✓		✓	✓	✓	✓	✓
	RapidIO-4	1.9-10	290	✓	✓	✓	✓	✓	✓		✓						✓	✓	✓		✓		✓	✓	✓	✓	✓
ITU / Telcordia	SONET/SDH OC-48	1-20	1000	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓		✓		✓	✓	✓	✓	✓
	SONET/SDH OC-192	4-20	240	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓		✓	✓	✓	✓	✓
	SONET/SDH OC-768	16-20	80															✓							✓		✓

Intel FPGA Phase Noise Mask Requirements

Stratix 10 GX/SX Arria 10 GX/SX/GT Stratix V GX/GS/GT Arria V GX/SX		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset	Phase Noise (156.25 MHz)	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x	Si5391	Si5341 Si5340	Si5332	Si539x	Si534x	Si5383/48
10 kHz	-112 dBc/Hz	-140 dBc/Hz	-132 dBc/Hz	-128 dBc/Hz	-136 dBc/Hz	-128 dBc/Hz	-140 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-126 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-137 dBc/Hz
100 kHz	-122 dBc/Hz	-145 dBc/Hz	-139 dBc/Hz	-135 dBc/Hz	-142 dBc/Hz	-133 dBc/Hz	-150 dBc/Hz	-146 dBc/Hz	-141 dBc/Hz	-132 dBc/Hz	-145 dBc/Hz	-141 dBc/Hz	-145 dBc/Hz
1 MHz	-132 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz	-144 dBc/Hz	-150 dBc/Hz	-144 dBc/Hz	-154 dBc/Hz	-149 dBc/Hz	-150 dBc/Hz	-154 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz

Arria V GT/ST		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset	Phase Noise (156.25 MHz)	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x	Si5391	Si5341 Si5340	Si5332	Si539x	Si534x	Si5383/48
10 kHz	-120 dBc/Hz	-140 dBc/Hz	-132 dBc/Hz	-128 dBc/Hz	-136 dBc/Hz	-128 dBc/Hz	-140 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-126 dBc/Hz	-136 dBc/Hz	-136 dBc/Hz	-137 dBc/Hz
100 kHz	-120 dBc/Hz	-145 dBc/Hz	-139 dBc/Hz	-135 dBc/Hz	-142 dBc/Hz	-133 dBc/Hz	-150 dBc/Hz	-146 dBc/Hz	-141 dBc/Hz	-132 dBc/Hz	-145 dBc/Hz	-141 dBc/Hz	-145 dBc/Hz
1 MHz	-130 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz	-144 dBc/Hz	-150 dBc/Hz	-144 dBc/Hz	-154 dBc/Hz	-149 dBc/Hz	-150 dBc/Hz	-154 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz	-150 dBc/Hz

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Offset	Phase Noise (156.25 MHz)	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x	Si5391	Si5341 Si5340	Si5332	Si539x	Si534x	Si5383/48
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100 kHz	-138 dBc/Hz	-145 dBc/Hz	-139 dBc/Hz	-135 dBc/Hz	-141 dBc/Hz	-133 dBc/Hz	-150 dBc/Hz	-146 dBc/Hz	-141 dBc/Hz	-132 dBc/Hz	-141 dBc/Hz	-141 dBc/Hz	-145 dBc/Hz
1 MHz	-140 dBc/Hz	-152 dBc/Hz	-151 dBc/Hz	-144 dBc/Hz	-150 dBc/Hz	-144 dBc/Hz	-154 dBc/Hz	-149 dBc/Hz	-160 dBc/Hz	-154 dBc/Hz	-160 dBc/Hz	-160 dBc/Hz	-160 dBc/Hz

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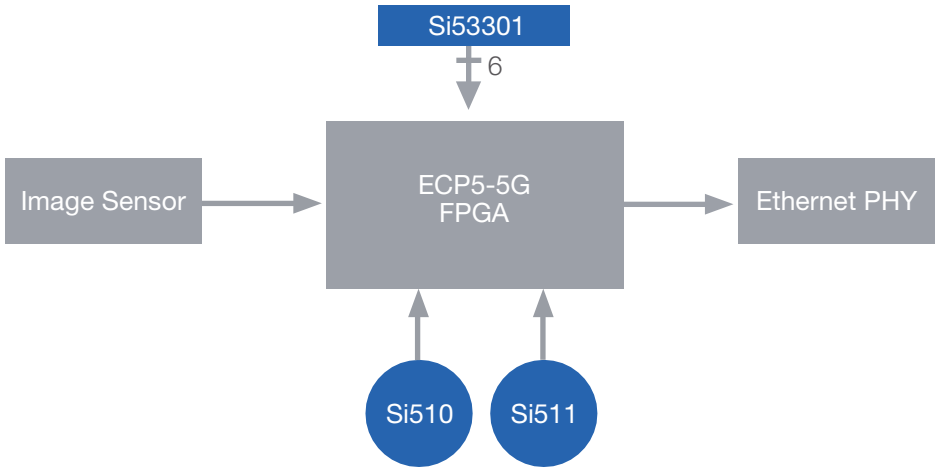

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- Ultra-low additive jitter: 50 fs RMS
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- Ultra-low jitter: 69 fs RMS
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Timing Solutions for Lattice Semiconductor

Silicon Labs			
Lattice Product Family	**Lattice Evaluation Board**	**Timing Requirement**	**Silicon Labs Recommended Device**
ECP5-5G	ECP5-5G Versa Board	1:6 Differential Buffer	Si53301
		100 MHz LVDS XO	Si511
		156.25 MHz CMOS XO	Si510
ECP5	ECP5 Evaluation Board	200 MHz LVDS XO	Si511
		50 MHz CMOS XO	Si510
ECP5	ECP5 VIP Processor Board	1:6 Differential Buffer	Si53301
		100 MHz LVDS XO	Si511
		125 MHz CMOS XO	Si510
ECP5-85	Crosslink Video Processing Input Board	1:2 CMOS buffer	Si53307
		27 MHz CMOS XO	Si510
		27 MHz CMOS XO	Si510
iCE40 UltraPlus	Crosslink Video Processing Input Board	27 MHz CMOS XO	Si510

For more information, visit www.silabs.com/timing

Request a custom clock or XO/VCXO at www.silabs.com/custom-timing

Silicon Labs

Timing Solutions for Marvell

Timing Simplified

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- Clock generators
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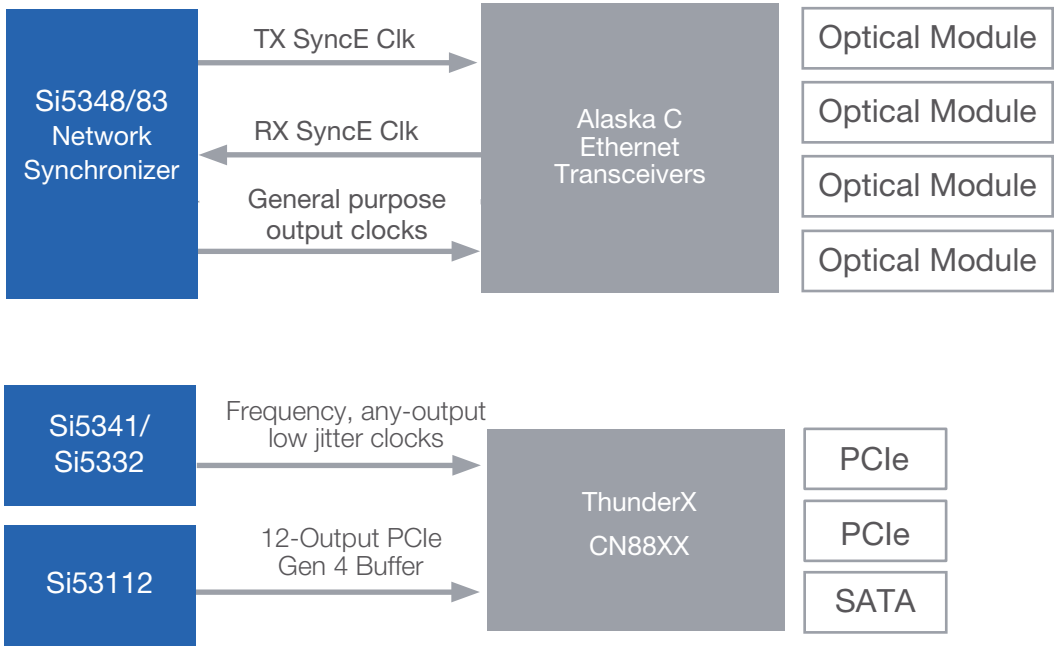
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.



For more information related to reference designs or partner pricing, please contact your local Silicon Labs sales representative.

Oscillators

- Any frequency up to 3 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs
- PCI Express Gen 1/2/3/4/5

Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Timing Solutions for Marvell

Silicon Labs							
Marvell Product Family	Marvell Part Number	XO	Clock Buffers	Clock Generators	Network Synchronizers/ Jitter Attenuating Clocks	PCIe Clocks	PCIe Buffers
Alaska C Ethernet Transceivers	88X7120 88X51xx	Si54x	Si5330x	Si5341 Si5391	Si5348	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
Alaska X 10 Gigabit Ethernet Transceivers	88X3xxx 88X2xxx	Si51x	Si5330x	Si5332	Si5348	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
Prestera CX Switches	98CX85xx	Si54x	Si5330x	Si5391	Si5348 Si539x	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
Prestera DX Switches	88DX8xxx 98DX4xxx 98DX3xxx	Si51x	Si5330x	Si5332	Si5348	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
Prestera EX Switches	98EX54xx	Si51x	Si5330x	Si5332	Si5348	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
Host Storage Controllers	88NV11xx 88SS109x 88SE9xxx	Si51x	Si5330x	Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
Printer SoCs	88PA6xxx	Si51x	Si5330x	Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
ThunderX ARM Processors	CN88XX CN87XX	Si54x	Si5330 Si5315 Si5311x	Si534x Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
ThunderX2 ARM Processors	CN99XX	Si54x	Si5330 Si5315 Si5311x	Si534x Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
OCTEON TX 64-bit ARM Processors	CN83XX CN82XX CN81XX CN80XX	Si54x	Si5330 Si5315 Si5311x	Si534x Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
OCTEON III Multi-Core MIPS64 Processors	CN7XXX CN78XX CN70XX	Si51x	Si5330 Si5315x Si5311x	Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
OCTEON II Multi-Core MIPS64 Processors	CN67XX CN66XX CN63XX CN62XX CN61XX	Si51x	Si5330 Si5315 Si5311x	Si5332	–	Si5214x (3.3V) Si522xx (1.5V, 1.8V)	Si5315x (3.3V) Si532xx (1.5V, 1.8V)
NITROX Security Processors	CNN55XX CNN35XX	Si51x	Si5330 Si5315 Si5311x	Si5332	–	–	–

For more information, visit www.silabs.com/timing

Request a custom clock or XO/VCXO at www.silabs.com/custom-timing

Silicon Labs

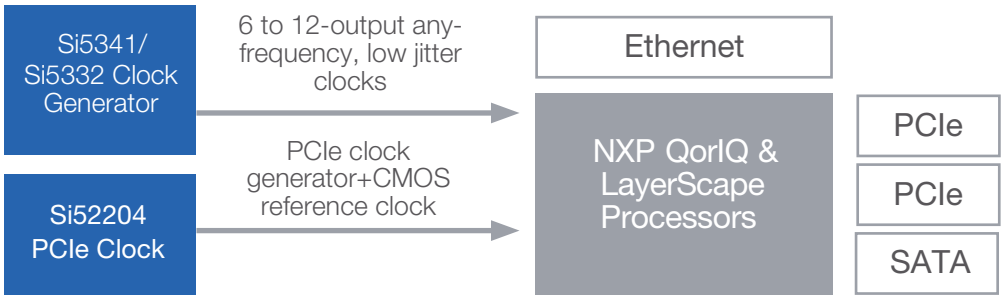
Timing Solutions for NXP QorIQ / LayerScape Processors

Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.



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Oscillators

- Any frequency up to 3.0 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs
- PCI Express Gen 1/2/3/4/5

Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Timing Solutions for QorIQ/LayerScape Processors

Application	NXP Part Number	Silicon Labs XO	Silicon Labs Clock Buffer		Silicon Labs Clock Generator	
			Multi-format outputs	PCIe	Multi-format outputs	PCIe
Telecom / Enterprise / Data Center Switches/routers Data center switches Storage Security	P10xx P20xx P30xx P40xx P50xx T10xx T20xx T4xxx LS10xx LS20xx LS21xx	Si54x	Si5330x	Si5135x	Si5431 Si5332	Si5214x Si5220x
Industrial Industrial switches, routers Motion control, robotics Medical imaging Defense and avionics Satcomm	P10xx P20xx T10xx T20xx	Si51x	Si5330x	Si5135x	Si5332 Si535x (CMOS only)	Si5214x Si5220x
Consumer	LS1012A LS1024A	Si51x	Si5330x	Si5135x	Si5332 Si535x (CMOS only)	Si5214x Si5220x

For more information, visit www.silabs.com/timing

Request a custom clock or XO/VCXO at www.silabs.com/custom-timing

Silicon Labs

Timing Solutions for Xilinx FPGAs

Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

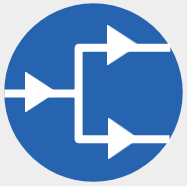
Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.

Oscillators

- Any frequency up to 3 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)

Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs



Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant

Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Recommended Timing Solutions for Xilinx

SILICON LABS

*Yes, but without spread spectrum
Note 1: Jitter integration band defined by jitter tolerance mask (receiver CDR) and XCVR PLL multiplying BW (20MHz default)
Note 2: Jitter defined by standard or as budgeted fraction of transmitter eye closure

Industry Standard Interface		Jitter Band [1] (MHz)	Max Jitter [2] (fs rms)	Xilinx										Silicon Labs											
				Versal		Kintex			Artix	Zynq	Virtex			XO/VCXO				Buffer		Clock Gen				Jitter Atten. Clock	
				AI Core & Prime	Premium	Ultra Scale+	Ultra Scale	7	7	Ultra Scale+	Ultra Scale+	Ultra Scale	7	Si51x	Si59x	Si54x	Si56x	Si533xx	Si532xx	Si522xx	Si5332	Si5341	Si5391	Si534x/8x	Si539x
OIF	CEI-6G-SR/LR	4-20	630	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
	CEI-11G-SR	8-20	380	✓	✓		✓	✓		✓	✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
	CEI-28G-VSR	16-20	150	✓	✓		✓	✓		✓	✓	✓	✓			✓	✓					✓	✓	✓	✓
	CEI-56G-PAM4-MR/LR	4-20	350	✓	✓						✓					✓	✓	✓			✓	✓	✓	✓	✓
	CEI-56G-PAM4-VSR	4-20	240	✓	✓						✓					✓	✓				✓	✓	✓	✓	✓
	CEI-112G-PAM4-VSR	4-20	120[3]		✓											✓	✓						✓		✓
	SFI-5.1	4-20	1300	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
	SFI-5.2	4-20	380	✓	✓		✓	✓		✓	✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
IEEE 802.3	1000BASE-X (GbE)	0.6-10	3000	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
	10GBASE-R	0.6-20	430	✓	✓		✓	✓	✓	✓	✓	✓				✓	✓	✓			✓	✓	✓		✓
	10GBASE-KR	0.6-20	430	✓	✓		✓	✓	✓	✓	✓	✓	✓			✓	✓	✓			✓	✓	✓	✓	✓
	400GAUI-8 C2C	4-20	380	✓	✓						✓					✓	✓	✓			✓	✓	✓	✓	✓
	400GAUI-8 C2M	4-20	275	✓	✓						✓					✓	✓	✓			✓	✓	✓	✓	✓
	CDAUI-16 (400GbE)	4-20	480	✓	✓					✓	✓				✓	✓	✓	✓			✓	✓	✓	✓	✓
	CDAUI-8 (400GbE)	4-20	240	✓	✓						✓					✓	✓				✓	✓	✓	✓	✓
	CAUI-4	1.9-10	280	✓	✓		✓	✓	✓	✓	✓	✓	✓			✓	✓	✓			✓	✓	✓	✓	✓
	CAUI-10	1.9-4	460	✓	✓		✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
	XAUI 10GBASE-X	0.6-20	430	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
	XLAUI (40GbE)	0.6-20	430	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
	OTN (OTU/EPON)	0.6-20	430	✓	✓		✓	✓		✓	✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
	SGMII/QSGMII	4-20	1400	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
Proprietary	RXAUI/DXAUI	1.9-20	950	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓

*Yes, but without spread spectrum
Note 1: Jitter integration band defined by jitter tolerance mask (receiver CDR) and XCVR PLL multiplying BW (20MHz default)
Note 2: Jitter defined by standard or as budgeted fraction of transmitter eye closure

Industry Standard Interface		Jitter Band [1] (MHz)	Max Jitter [2] (fs rms)	Xilinx										Silicon Labs											
				Versal		Kintex			Artix	Zynq	Virtex			XO/VCXO				Buffer		Clock Gen				Jitter Atten. Clock	
				AI Core & Prime	Premium	Ultra Scale+	Ultra Scale	7	7	Ultra Scale+	Ultra Scale+	Ultra Scale	7	Si51x	Si59x	Si54x	Si56x	Si533xx	Si532xx	Si522xx	Si5332	Si5341	Si5391	Si534x/8x	Si539x
ITU	GPON	0.6-10	1500	✓	✓		✓	✓			✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
CPRI	CPRI 10G	various	Various 10G+	✓	✓		✓	✓	✓		✓	✓	✓			✓	✓	✓			✓	✓	✓	✓	✓
	CPRI 12G	various	Various 12G+	✓	✓		✓	✓	✓		✓	✓	✓			✓	✓	✓			✓	✓	✓	✓	✓
	CPRI 24G	various	Various 24G+	✓	✓		✓	✓	✓		✓	✓	✓			✓	✓	✓				✓	✓	✓	✓
ANSI	Fibre Ch – 8G, 16G	0.6-10	240	✓	✓		✓	✓	✓		✓	✓	✓			✓	✓	✓			✓	✓	✓	✓	✓
	Fibre Ch – 32G	0.6-10	130	✓	✓		✓	✓	✓		✓	✓	✓			✓	✓					✓	✓	✓	✓
JEDEC	JESD204B	various	Per DAC/ADC	✓	✓		✓	✓	✓		✓	✓	✓									✓	✓	✓	✓
Intel	Interlaken – 6G	4-20	630	✓	✓		✓	✓			✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
	Interlaken – 10G	4-20	380	✓	✓		✓	✓			✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
	QPI	Intel	200	✓	✓		✓	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI-SIG	PCI Express Gen3	various	1000	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	*	*	*	*	✓	✓	✓	✓	*	*	*	*
	PCI Express Gen4	various	500	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	*	*	*	*	✓	✓	✓	✓	*	*	*	*
	PCI Express Gen5	various	150	✓	✓									*	*	*	*	✓	✓	✓	✓	*	*	*	*
CCIX	CCIX-25G	various	350	✓	✓									*	*	*	*	✓	✓		✓	*	*	*	*
SATA-IO	SAS/SATA 6G	2.6-15	780	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
	SAS/SATA 12G	2.6-15	390	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
SMPTE	SDI 3G, 6G	0.1-F/2	800	✓	✓		✓	✓	✓		✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
	SDI 12G	0.1-F/2	400	✓	✓		✓	✓	✓		✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
	SDI 24G	0.1-F/2	200	✓	✓						✓					✓						✓	✓	✓	✓
RapidIO	RapidIO-1, -2, -3	4-20	410	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓
	RapidIO-4	1.9-10	290	✓	✓		✓	✓	✓		✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
ITU ANSI	SONET/SDH OC-48	1-20	1000	✓	✓		✓	✓			✓	✓	✓	✓		✓	✓	✓			✓	✓	✓	✓	✓
	SONET/SDH OC-192	4-20	240	✓	✓		✓	✓			✓	✓	✓		✓	✓	✓	✓			✓	✓	✓	✓	✓
	SONET/SDH OC-768	16-20	80	✓	✓											✓							✓		✓

Xilinx UltraScale+ Phase Noise Mask Requirements

Xilinx Virtex, Kintex UltraScale+ GTH Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 Hz	-111	-140	-132	-129	-130	-128	-140	-136	-136	-125	-136	-136	-137
100 kHz	-130	-145	-139	-134	-142	-133	-150	-146	-141	-132	-141	- 145	-145
1 MHz	-136	-152	-151	-145	-150	-144	-154	-150	-150	-145	-150	-150	-150

Xilinx Zync Ultrascale+ GTH Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 kHz	-111	-140	-132	-129	-130	-132	-140	-136	-136	-125	-136	-136	-137
100 kHz	-130	-145	-139	-134	-142	-142	-150	-146	-141	-132	-141	- 145	-145
1 MHz	-136	-152	-151	-145	-150	-148	-154	-150	-150	-145	-150	-150	-150

Xilinx UltraScale Phase Noise Mask Requirements

Xilinx Virtex, Kintex UltraScale+ GTY Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 Hz	-112	-140	-132	-129	-130	-128	-140	-136	-136	-125	-136	-136	-137
100 kHz	-128	-145	-139	-134	-142	-133	-150	-146	-141	-132	-141	-145	-145
1 MHz	-145	-152	-151	-145	-150	-144	-154	-150	-150	-145	-150	-150	-150

Xilinx Zync Ultrascale+ GTY Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 kHz	-112	-140	-132	-129	-130	-132	-140	-136	-136	-125	-136	-136	-137
100 kHz	-128	-145	-139	-134	-142	-142	-150	-146	-141	-132	-141	-145	-145
1 MHz	-145	-152	-151	-145	-150	-148	-154	-150	-150	-145	-150	-150	-150

Xilinx UltraScale Phase Noise Mask Requirements

Xilinx Virtex, Kintex UltraScale+ GTM Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 Hz	-112	-140	-132	-129	-130	-128	-140	-136	-136	-125	-136	-136	-137
100 kHz	-130	-145	-139	-134	-142	-133	-150	-146	-141	-132	-141	-145	-145
1 MHz	-145	-152	-151	-145	-150	-144	-154	-149	-149	-145	-150	-150	-150

Xilinx Zync Ultrascale+ GTM Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 kHz	-111	-140	-132	-129	-130	-132	-140	-136	-136	-125	-136	-136	-137
100 kHz	-130	-145	-139	-134	-142	-142	-150	-146	-141	-132	-141	-145	-145
1 MHz	-136	-152	-151	-145	-150	-148	-154	-149	-149	-145	-150	-150	-150

Xilinx UltraScale Phase Noise Mask Requirements

Xilinx Virtex, Kintex Ultrascale GTH Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 kHz	-111	-140	-132	-129	-130	-132	-140	-136	-136	-125	-136	-136	-137
100 kHz	-130	-145	-139	-134	-142	-142	-150	-146	-141	-132	-141	-145	-145
1 MHz	-136	-152	-151	-145	-150	-148	-154	-150	-150	-145	-150	-150	-150

Xilinx Virtex, Kintex Ultrascale GTY Transceiver		XO			VCXO		Clock Buffer	Clock Generator			Jitter Attenuating Clock		Network Synchronizers (SyncE/1588)
Offset (dBc/Hz)	QPLL PN 156.25 MHz	Si545	Si540	Si570/ Si53x	Si56x	Si55x	Si5330x Universal Buffers	Si5391	Si5341 Si5340	Si5332	Si5347/6/5/4/2	Si5392/5	Si5383/48
10 kHz	-112	-140	-132	-129	-130	-132	-140	-136	-136	-125	-136	-136	-137
100 kHz	-128	-145	-139	-134	-142	-142	-150	-146	-141	-132	-141	-145	-145
1 MHz	-145	-152	-151	-145	-150	-148	-154	-150	-150	-145	-150	-150	-150

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