Application Note Software

Li-Ion Battery Monitoring and Balancing IC

About this document

Application Note to develop software for multi-cell monitoring and balancing ICs TLE9012AQU & TLE9015QU designed for Li-ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in stationary Lithium-Ion batteries.

Note: *The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

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1 Initialization

In order to be able to communicate with the TLE9012AQU slave ICs in the daisy chain, a CONFIG.NODE_ID (0x36) must be assigned to them. Before the initialization, the NODE_ID of all slaves in the chain is ID=0x00. If the NODE_ID=0x00, no iso UART frames are forwarded to the next slave in the chain.

The following frame sequence shows an example initialization of four slaves in a chain. The daisy chain is connected to the low-side iso UART interface of the TLE9015QU transceiver (see **Figure 1**).

Table 1 Initialize first IC with NODE_ID=0x01

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x80	MSB=1 indicated a write command; 6 Bit device ID =0b000000.
Addr	0x36	Address of CONFIG register.
Data	0x0001	Assigns NODE_ID=0x01 to the first slave in the chain.
CRC	0x78	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

From this point onwards, the slave closest to the transceiver IC has the NODE_ID=0x01 and forwards the messages. Now the next slave in the chain corresponds to NODE_ID=0x00 and the process shall be repeated (see below).

Note: The watchdog for NODE_ID=0x01 must be triggered if the initialization process takes longer than the predefined watchdog timer (WDOG_CNT.WD_CNT). Otherwise, the slave will go to sleep mode and resets the NODE_ID to 0 again.

Table 2 Initialize second IC with NODE_ID=0x02

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x80	MSB=1 indicated a write command; 6 Bit device ID =0b000000.
Addr	0x36	Address of CONFIG register.
Data	0x0002	Assigns NODE_ID=0x02 to the second slave in the chain.
CRC	0x09	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

From this point onwards, the second slave has NODE_ID=0x02, therefore the same applies as above for IC #1.

Table 3 Initialize third IC with NODE_ID=0x03

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x80	MSB=1 indicated a write command; 6 Bit device ID =0b000000.
Addr	0x36	Address of CONFIG register.
Data	0x0003	Assigns NODE_ID=0x03 to the third slave in the chain.
CRC	0x26	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

From this point onwards, the third slave has NODE_ID=0x03, therefore the same applies as above for IC #1.

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Table 4 Initialize forth IC with NODE_ID=0x04

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x80	MSB=1 indicated a write command; 6 Bit device ID =0b000000.
Addr	0x36	Address of CONFIG register.
Data	0x0804	Final Node FN=1, otherwise no reply frame will be sent on broadcast -> iso UART time-out. NODE_ID=0x04 assigned to the fourth slave in the chain.
CRC	0x6E	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

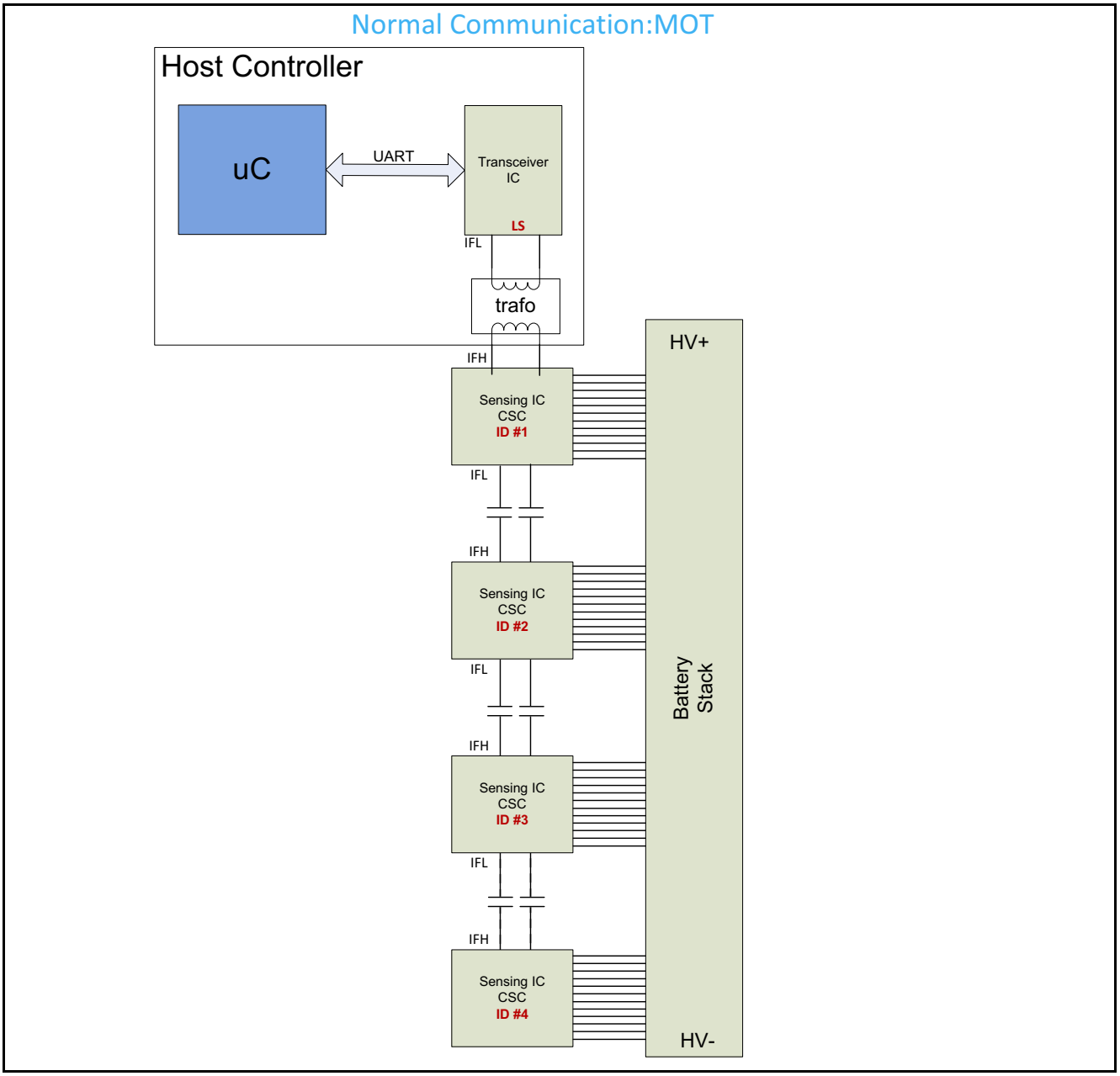

Figure 1 Master-on-Top application (wake-up via low-side interface)

1.1 CRC

The CRC for the CRC frame is calculated according to the following equation:

(1.1)

$$G[z] = z8 + z5 + z3 + z2 + z + 1$$

1.2 Read back of configuration registers

The microcontroller shall read back the register content after writing to a configuration register to check if the data writing was correct.

The following example shows the read back of the CONFIG (0x36) register:

Table 5 Read back CONFIG register of the first IC

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x01	MSB=0 indicated a read command; 6 Bit device ID =0b000001.
Addr	0x36	Address of CONFIG register.
CRC	0x62	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

2 Configuration

2.1 Partitioning config

The PART_CONFIG (0x01) register defines how many cells are connected to the sensing IC. This register determines which ADCs are activated during the cell voltage measurement (CVM) and checked during the round robin scheme.

The following frame sequence activates all 12 CVM channels for the slave with the NODE_ID=1:

Table 6 PART_CONFIG

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x01	Address of PART_CONFIG register.
Data	0x0FFF	Enables cell monitoring for all 12 cells.
CRC	0xC1	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

*Note: Generally, this command can be sent as a broadcast write command if it shall affect all IC's in the daisy chain. This applies for all other registers as well. An example for a broadcast write command is shown in **Table 14**.*

2.2 Cell voltage thresholds

The cell voltages can be check via comparators and a digital-to-analog converter (DAC). The thresholds for the comparator are configured in the overvoltage OL_OV_THR (0x02) and undervoltage OL_UV_THR (0x03) registers.

The following frame sequence configures an undervoltage threshold of e.g. 1.5 V and an overvoltage threshold of e.g. 4.6 V for the first slave:

Table 7 Overvoltage OL_OV_THR set to 4.6 V

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x02	Address of OL_OV_THR register.
Data	0xFFAE	Set OL_OV_THR.OV_THR=0x3AE Calculation: 4.6V / (FSR/10bit) = 4.6V / (5V/1024) default value for OL_THR_MAX used.
CRC	0x48	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

Table 8 Overvoltage OL_UV_THR set to 1.5 V

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x03	Address of OL_UV_THR register.
Data	0x0134	Set OL_UV_THR.UV_THR=0x134 Calculation: 1.5V / (FSR/10bit) = 1.5 V / (5V/1024) default value for OL_THR_MIN used.
CRC	0x53	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

2.3 Open load diagnosis

The open load diagnosis offers the possibility to automatically detect open wires. Therefore, the open load thresholds needs to be set to define the minimum and maximum voltage drop while OL-diagnosis.

The configuration of the thresholds depends on the used filter resistor, e.g. with the recommended filter resistor of 5.1Ω and I_{OL_DIAG} (min. 10mA, max. 18.3mA), the min. voltage drop is 0.051V (= 5.1Ω*10mA) and the max. voltage drop is 0.093V (=5.1Ω*18.3mA). To prevent false triggering of the OL error (due to noise), an additional buffer can be added e.g. 30mV.

The following frame sequences sets the OL_OV_THR.OL_THR_MAX=0.123V and the OL_UV_THR.OL_THR_MIN=0.021V for the first slave IC:

Table 9 Openload maximum voltage drop threshold OL_THR_MAX=0.123V

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.

Configuration

Table 9 Openload maximum voltage drop threshold OL_THR_MAX=0.123V

Frame-Type	Value	Comment
Addr	0x02	Address of OL_OV_THR register.
Data	0x67FF	Set OL_OV_THR.OL_THR_MAX=0b011001 Calculation: 0.123V / (FSR/10bit) = 0.123V / (5V/1024) default value for OV_THR used.
CRC	0x88	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

Table 10 Openload minimum voltage drop threshold OL_THR_MIN=0.021V

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x03	Address of OL_UV_THR register.
Data	0x1000	Set OL_UV_THR.OL_THR_MIN=0b000100 Calculation: 0.021V / (FSR/10bit) = 0.021V / (5V/1024) default value for UV_THR used.
CRC	0xF0	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

2.4 NTC Temperature measurement configuration

The TLE9012AQU can measure up to 5 external temperature sensors. As part of the round robin (RR) scheme, up to two temperature measurements can be performed in every RR cycle.

The number of external temperature sensors is configured in the TEMP_CONF (0x04) register. As an example, all temperature channels are activated for slave 1:

Table 11 Number of external temperature sensors NR_TEMP_SENSE

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x04	Address of TEMP_CONF register.
Data	0x5000	Set TEMP_CONF.NR_TEMP_SENSE=0b101; default values for I_NTC and EXT_OT_THR used.
CRC	0x40	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

2.5 Balancing current thresholds

A balancing overcurrent (OC_THR) or undercurrent (UC_THR) check is done during the round robin cycle. If the balancing current is lower than the UC_THR or higher than the OC_THR, the corresponding error counter will be incremented.

The example shows a threshold configuration for slave 1 with a max. balancing current I_{BAL} = 4.3V /(5.1+28+1.5)Ω = 124mA at 4.3V and a min. balancing current I_{BAL} = 2.7V / (5.1+28+5.3)Ω = 70.3mA at 2.7V. A filter resistor R_F of 5.1Ω and a balancing resistor of 28Ω is assumed and the balancing switch on-state resistance R_{BAL_DSON} is considered.

Cell voltage measurement

A voltage of +/-100mV is used as voltage drop (I_{BAL}*R_F) buffer, the balancing current voltage drop must be within min. (0.0703A* 5.1Ω - 0.1V) = 0.259V and max. (0.124A * 5.1Ω + 0.1V) = 0.732V.

Table 12 Balancing current thresholds BAL_CURR_THR (0x15)

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x15	Address of BAL_CURR_THR register.
Data	0x3596	Set BAL_CURR_THR.UC_THR=0b00110101, Calculation: (typ. 0.259V / (FSR/10bit) = 0.259V / (5V/1024) Set BAL_CURR_THR.OC_THR=0b10010110, Calculation: (typ. 0.732V / (FSR/10bit) = 0.732V / (5V/1024)
CRC	0xE3	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

3 Cell voltage measurement

To initiate a cell voltage measurement of the connected cells, the bit-field MEAS_CTRL.CVM_START needs to be set. The measurement starts after the programmable delay time t_{CVM_del}. The delay time enables the external filter to settle to e.g. avoid errors due to prior balancing. t_{CVM_del} is active independent of the balancing status. After the measurement, the CVM_START bit-field is automatically cleared and the result is available in the CVM0 - CVM_11 result registers. The CVM0 - CVM_11 registers will be reset during the measurement until the measurement is finished. To avoid measurement errors due to passive balancing current, the PBOFF bit-field is by default “1” to automatically deactivate the passive balancing switches during the cell voltage measurement.

The following example shows the initiation of the cell voltage measurement with 16 bit for slave 1:

Table 13 Measurement control MEAS_CTRL (0x18)

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x18	Address of MEAS_CTRL register.
Data	0xE021	Set CVM_START=1, Set CVM_BIT_WIDTH=0b110 (16 bit), default for BVM, AVM, PBOFF, CVM_DEL (see datasheet)
CRC	0xDC	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

A broadcast write command can be used to start the measurement for all ICs in the chain at the same time. The following example starts the voltage measurements for IC #1 to IC #4 (see **Figure 1**):

Table 14 Broadcast write to measurement control MEAS_CTRL (0x18)

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0xBF	MSB=1 indicated a write command; 6 Bit device ID =0b111111 indicate a broadcast command.
Addr	0x18	Address of MEAS_CTRL register.
Data	0xE021	Set CVM_START=1, Set CVM_BIT_WIDTH=0b110 (16 bit), default for BVM, AVM, PBOFF, CVM_DEL
CRC	0xB2	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

4 Block voltage measurement

The 13th ADC can perform different auxiliary voltage measurements including a block voltage measurement (BVM). The voltage is measured between U12P and GND. A BVM measurement is initiated by setting the bit-field MEAS_CTRL.BVM_START and starts after t_{BVM_prop}. The measurement result is stored in the BVM (0x28) register and the BVM_START bit is automatically cleared after the measurement.

The following example shows the initiation of the block voltage measurement with 16 bit for slave 1:

Table 15 Measurement control MEAS_CTRL (0x18)

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x18	Address of MEAS_CTRL register.
Data	0x0E21	Set BVM_START=1, Set BVM_BIT_WIDTH=0b110 (16 bit), default for CVM, AVM, PBOFF, CVM_DEL
CRC	0xA8	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

5 Calculations

5.1 Voltage - CVM, BVM

After a cell voltage measure command (CVM), an unsigned value is stored in the RESULT bit-fields of the CVM_0 - CVM_11 (Offset Address: 0x19-0x24) registers. The equation to calculate the cell voltage is:

(5.1)

$$\mathrm{Cellvoltage[mV]} = (\mathrm{FSR} \times 1000\mathrm{[mV]}/(2^{16})) \times \mathrm{RESULT}$$

e.g. CVM_0 = 0xABCD

(5.2)

$$(5\mathrm{V} \times 1000[\mathrm{mV}]/(2^{16})) \times 0\mathrm{xABCD} \;=\; 3.355\mathrm{V}$$

Using the formula **Equation (5.1)**, a voltage of 3.355 V for cell 0 (CVM_0) is calculated.

To calculate the block voltage (BVM) after a block voltage measurement, a similar formula is used. The RESULT stored in the BVM register (Offset Address: 0x28) is converted to a voltage used the **Equation (5.3)**.

(5.3)

$$\mathrm{Blockvoltage}[\mathrm{mV}] \;=\; (\mathrm{FSR} \times 1000[\mathrm{mV}]/(2^{16})) \times \mathrm{RESULT}$$

e.g. BVM = 0xABCD

(5.4)

$$(60\mathrm{V} \times 1000[\mathrm{mV}]/(2^{16})) \times 0\mathrm{xABCD} \;=\; 40.266\mathrm{V}$$

Using the formula **Equation (5.3)**, a voltage of 40.266 V for the block voltage is calculated.

5.2 NTC Temperature

The results of the NTC temperature measurement are stored in the EXT_TEMP_0 - EXT_TEMP_4 (0x29 - 0x2D) registers.

The NTC resistor value is calculated with the following **Equation (5.5)**:

(5.5)

$$(\mathrm{RNTC})[\Omega] \;=\; (\mathrm{RESULT}[\mathrm{LSB10}] \times \mathrm{FSR}[\mathrm{V}] \times 4^{\mathrm{INTC}})/(2^{10} \times 320\mu\mathrm{A}) - \mathrm{R_{TMP}}$$

with INTC = 0 .. 3 (used current source).

e.g. EXT_TEMP_0 = 0x2747 (RESULT[LSB10] = 0x347 = 839; INTC=0x1)

(5.6)

$$(\mathrm{RESULT}[\mathrm{LSB10}] \times \mathrm{FSR}[\mathrm{V}] \times 4^{\mathrm{INTC}})/(2^{10} \times 320\mu\mathrm{A}) - \mathrm{R_{TMP}} \;=$$
$$(839 \times 2\mathrm{V} \times 4^{1})/(2^{10} \times 320\mu\mathrm{A}) - 100\Omega \;=\; 20.4\mathrm{k}\Omega$$

6 Balancing

Passive balancing can be activated to equalize the voltage levels of the connected battery cells. In the configuration register BAL_SETTINGS (0x16), the cells to be balanced can be selected in any combination including for all channels at the same time. To automatically switch off balancing during a CVM measurement and to delay the CVM measurement after balancing, see **Chapter 3**.

To select all 12 cell for the first TLE9012AQU in the chain, the following sequence must be send:

Balancing

Table 16 Write to Register BAL_SETTINGS (0x16)

Frame-Type	Value	Comment
Synch	0x1E	Fixed synchronization frame; necessary to start the communication with a defined scheme.
ID	0x81	MSB=1 indicated a write command; 6 Bit device ID =0b000001.
Addr	0x16	Address of BAL_SETTINGS register.
Data	0x0FFF	Set BAL.SETTINGS=0x0FFF to switch on the balancing drivers for cell 0 - 11.
CRC	0x0B	CRC-code is based on 8 Bit polynomial shown in **Equation (1.1)**.

7 Revision History

Revision	Date	Changes
1.0	2020-06-16	Initial Version

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