# **Do Systems Need SRAMs?**

## By Mark Baumann Director, Product Definition & Applications MoSys, Inc.

I am asking this question because it is my impression that the manufacturers of SRAMs like Cypress (Infineon) and GSI, are not demonstrating newer devices on their roadmaps. Even at MoSys, we understand that larger companies such as Intel, Xilinx and Cisco are looking at FPGAs. They are doing so either to incorporate whatever RAM resource that they can place on die or for ASICs to also place large RAM resources on die when possibly or as a third option to develop MCMs that have silicon such as HBM to mate with FPGAs or ASICs at the die level.

In the past, the criteria that was used to define if a block of SRAM or DRAM or another form of data storage was needed was resolved by a series of questions:

- How much data must be stored?
- For how long?
- Does the data need random access or purely sequential access?
- How fast must the data be accessed?

Each of these are issues need to be addressed when choosing the storage element that fits best, in a system.

## Amount (How Much?)

When considering the amount of data, the main factor that is considered is speed at which data is being received or disseminated. (Present SRAMs are in the 144Mb to 288Mb density and DRAMs are in the 64MB range or 2x SRAM, but in a package that is half the size of SRAM). Knowing the chip density, it is possible to examine the amount of storage needed to meet system requirements. For example, if interfacing to a 100G ethernet port one MoSys BE-2 device (a 576Mb MoSys device) can absorb close to 6us of full-bandwidth data, if this is a requirement of your system. Or, if a slower store and forward access to memory is needed and could be handled by DRAM or HBM.

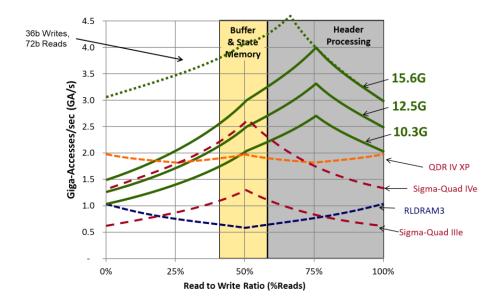
| Metric                 | Vs. SRAM<br>S.Q. or QDR<br>III | Vs. SRAM<br>S.Q. or QDR<br>IV | Vs.<br>RLDRAM3 | Vs.<br>DRAM |
|------------------------|--------------------------------|-------------------------------|----------------|-------------|
| Access Rate            | 4x                             | 2X                            | 6x             | 40x         |
| Density                | 4x                             | 4x                            | 1X             | 1/4 X       |
| Latency                | 1/4 X                          | 1⁄2 X                         | 1X             | 4x          |
| Bandwidth              | 4x                             | 3x                            | 6x             | 8x          |
| Pin-count              | 2X                             | 2X                            | 1X             | 1/2 X       |
| Power                  | 1/2 X                          | 1⁄2 X                         | 1/3 x          | 1/10 x      |
| Effective<br>Advantage | 16x                            | 13x                           | 12x            | 16x         |

## **How Long**

If data is just being absorbed and held onto for any length of time it may be more cost effective and efficient to utilize a bulk storage like DRAM. However, if data is just flowing through at line rate there is a real benefit to SRAM like performance that can "keep up" with the associated line rate. Otherwise, there can be penalties to the system if slower access like DRAM causes the needs to buffering data while clearing some form of "head of line blockage".

#### **Random Access**

SRAM devices are ideally designed for fast random-access environments. The design of the device allows for high speed random access and is different than a DRAM. Even though a DRAM can achieve very high bandwidth it does so when access data that is sequential, and not random. In environments such as table lookups where requests are purely random, SRAM – Random access is required. DRAM access to random locations can take up to 10x longer than SRAM and this can have a direct impact on system throughput.



#### Access Speed

As mentioned in the previous paragraph, RAM devices either Static or Dynamic, allow for Read and Write Access to storage cells. The significant difference is that Static devices are designed for faster access than Dynamic. Dynamic cells are designed for small size to allow for dense packing and large amounts of storage.

Most present-day systems require a combination of both. Certainly, large amounts of data is being shared through networks at ever increasing speeds. So, bulk storage is becoming more important. So is the speed at which decisions need to be made, for

routing, security, and even finance, which enhances the importance of high-speed random-access memory.

## **Conclusion:**

Just as with most things we encounter, there is no simple or easy answer to the question of what storage elements are needed. But the reality is that SRAM type memory IS NEEDED and is increasing in importance as the speed of systems increase. MoSys has developed the next generation, denser and higher bandwidth random-access memory, to address this need.

If your design requires a denser, higher bandwidth, Random-access memory please visit mosys.com and see how these Bandwidth Engine devices can help in addressing your memory issues.

#### **Additional Resources:**

Packet Classification Platform What is a Virtual Accelerator? Webinar EETimes-MoSys Virtualized Acceleration: The MoSys Approach Press Releases MoSysBandwidthengine Vs.QDR The Benefits of Serial Memory FPGA and Memory Latency

If you are looking for more technical information or need to discuss your technical challenges with an expert, we are happy to help. <u>Email us</u> and we will arrange to have one of our technical specialists speak with you. You can also sign up for <u>updates</u>. Finally, please follow us on social media so we can keep in touch.

