Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs

By Glenn Morita

Low-dropout regulators (LDOs) are deceptively simple devices that provide critical functions such as isolating a load from a dirty source or creating a low-noise source to power sensitive circuitry.

This brief tutorial introduces some common terms used with LDOs, explaining fundamental concepts such as dropout voltage, headroom voltage, quiescent current, ground current, shutdown current, efficiency, dc line-and-load regulation, transient line-and-load response, power-supply rejection ratio (PSRR), output noise, and accuracy, using examples and plots to make them easy to understand.

LDOs are often selected late in the design process with little analysis. The concepts presented here will enable designers to select the best LDO based on system requirements.

Dropout Voltage

Dropout voltage ($V_{DROPOUT}$) is the input-to-output voltage difference at which the LDO is no longer able to regulate against further decreases in the input voltage. In the dropout region, the pass element acts like a resistor with a value equal to the drain-to-source on resistance (RDS_{ON}). The dropout voltage, expressed in terms of RDS_{ON} and load current, is

$$V_{DROPOUT} = I_{LOAD} \times RDS_{ON}.$$

RDS_{ON} includes resistance from the pass element, on-chip interconnects, leads, and bond wires, and can be estimated by the LDO's dropout voltage. For example, the ADP151 in the WLCSP has a worst-case dropout voltage of 200 mV with a 200-mA load, so the RDS_{ON} is about 1.0 Ω. Figure 1 shows a simplified schematic of an LDO. In dropout, the variable resistance is close to zero. The LDO cannot regulate the output voltage, so other parameters such as line-and-load regulation, accuracy, PSRR, and noise are meaningless.

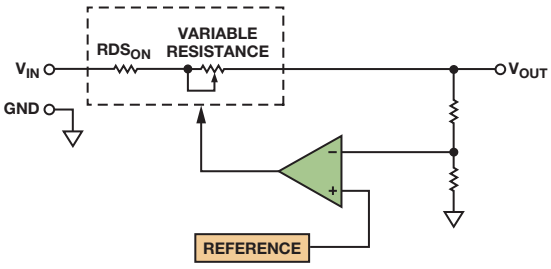

Figure 1. Simplified schematic of an LDO.

Figure 2 shows the output voltage vs. input voltage of the 3.0-V ADM7172 LDO. The dropout voltage is typically 172 mV at 2 A, so RDS_{ON} is about 86 mΩ. The dropout region extends from about 3.172 V input voltage down to 2.3 V. Below 2.3 V, the device is nonfunctional. At smaller load currents, the dropout voltage is proportionately lower: at 1 A, the dropout voltage is 86 mV. A low dropout voltage maximizes the regulator's efficiency.

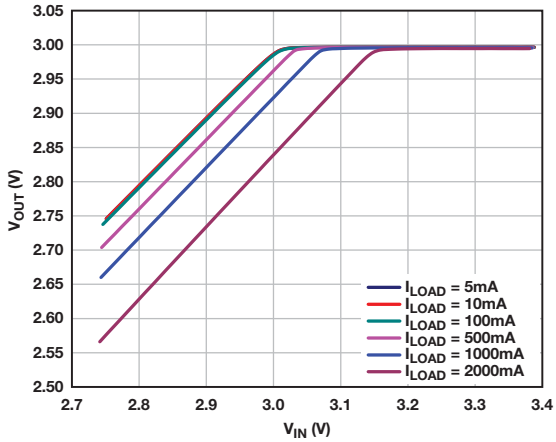

Figure 2. Dropout region of the 3.0-V ADM7172 LDO.

Headroom Voltage

Headroom voltage is the input-to-output voltage difference required for an LDO to meet its specifications. The data sheet usually shows the headroom voltage as the condition at which the other parameters are specified. The headroom voltage is typically around 400 mV to 500 mV, but some LDOs require as much as 1.5 V. Headroom voltage should not be confused with dropout voltage, as they are the same only when the LDO is in dropout.

Quiescent and Ground Current

Quiescent current (I_Q) is the current required to power the LDO's internal circuitry when the external load current is zero. It includes the operating currents of the band-gap reference, error amplifier, output voltage divider, and overcurrent and overtemperature sensing circuits. The amount of quiescent current is determined by the topology, input voltage, and temperature.

$$I_Q = I_{IN} \text{ @ no load}$$

The quiescent current of the ADP160 LDO is nearly constant as the input voltage varies between 2 V and 5.5 V, as shown in Figure 3.

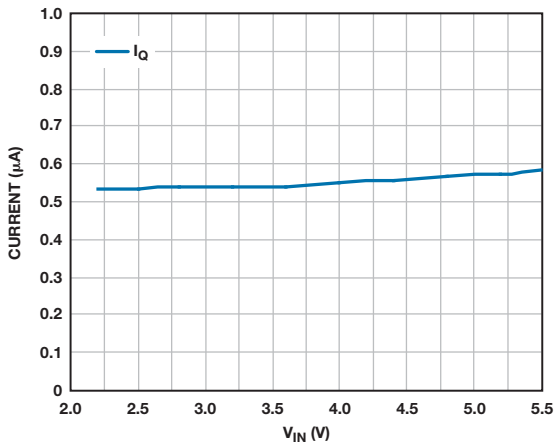

Figure 3. Quiescent current vs. input voltage of the ADP160 LDO.

Ground current (I_{GND}) is the difference between the input and output currents, and necessarily includes the quiescent current. A low ground current maximizes the LDO efficiency.

$$I_{GND} = I_{IN} - I_{OUT}$$

Figure 4 shows the ground current variation vs. load current for the ADP160 LDO.

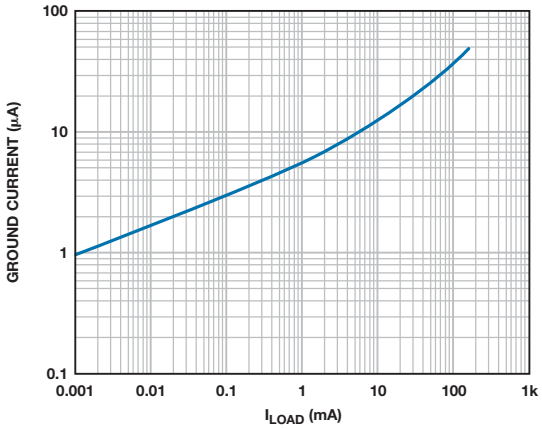

Figure 4. Ground current vs. load current of the ADP160 LDO.

For high-performance CMOS LDOs, the ground current is typically much less than 1% of the load current. Ground current increases with load current because the gate drive to the PMOS pass element must increase to compensate for the voltage drop caused by its R_{ON}. In the dropout region, the ground current can also increase as the driver stage starts to saturate. CMOS LDOs are essential in applications where low power consumption or small bias currents are critical.

Shutdown Current

Shutdown current is the input current drawn by the LDO when the output is disabled. The reference and error amplifier are not powered in shutdown mode. Higher leakage currents cause the shutdown current to increase with temperature, as shown in Figure 5.

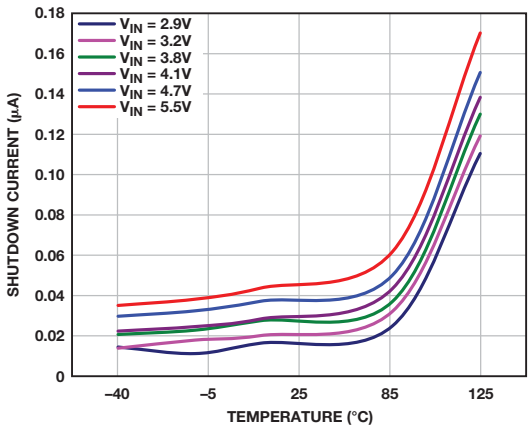

Figure 5. Shutdown current vs. temperature of the ADP160 LDO.

Efficiency

The efficiency of an LDO is determined by the ground current and input/output voltages:

$$\text{Efficiency} = I_{OUT}/(I_{OUT} + I_{GND}) \times V_{OUT}/V_{IN} \times 100\%$$

For high efficiency, the headroom voltage and ground current must be minimized. In addition, the voltage difference between input and output must be minimized. The input-to-output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions. For example, the efficiency of a 3.3-V LDO will never exceed 66% when powered from 5 V, but it will rise to a maximum of 91.7% when the input voltage drops to 3.6 V. The power dissipation of an LDO is $(V_{IN} - V_{OUT}) \times I_{OUT}$.

DC Load Regulation

Load regulation is a measure of the LDO's ability to maintain the specified output voltage under varying load conditions. Load regulation, shown in Figure 6, is defined as

$$\text{Load regulation} = \Delta V_{OUT}/\Delta I_{OUT}$$

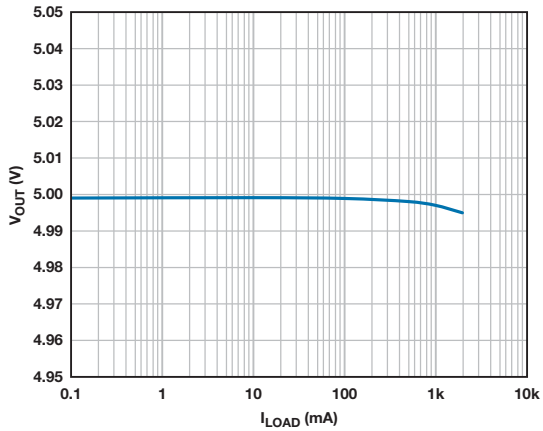

Figure 6. Output voltage vs. load current for the ADM7172 LDO.

DC Line Regulation

Line regulation is a measure of the LDO's ability to maintain the specified output voltage with varying input voltage. Line regulation is defined as

$$\text{Line regulation} = \Delta V_{OUT}/\Delta V_{IN}.$$

Figure 7 shows the output voltage of the ADM7172 vs. input voltage at different load currents. The line regulation gets worse as the load current increases because the LDO's overall loop gain decreases. Also, the LDO's power dissipation increases as the input-to-output voltage differential increases. This causes the junction temperature to rise and in this case, the band-gap voltage and internal offset voltages to decrease.

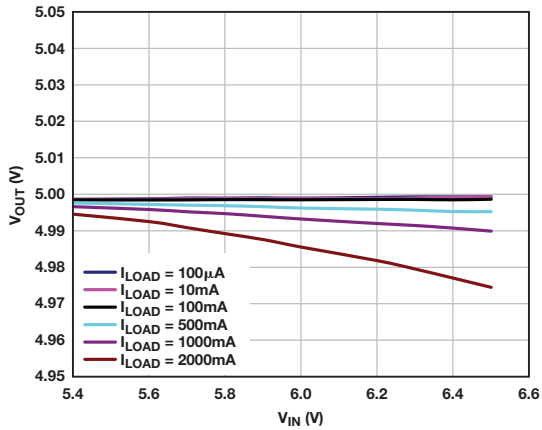

Figure 7. Output voltage vs. input voltage for the ADM7172 LDO.

DC Accuracy

The overall accuracy considers the effects of line-and-load regulation, reference voltage drift, and error amplifier voltage drift. The output voltage variation in a regulated power supply is due primarily to temperature variation of the reference voltage and the error amplifier. If discrete resistors are used to set the output voltage, the tolerance of the resistors may well be the largest contributor to overall accuracy. Line-

and-load regulation and error amplifier offsets normally account for 1% to 3% of the overall accuracy.

For example, calculate the total accuracy of a 3.3-V LDO over the 0°C to 125°C temperature span with the following operating characteristics: ±100 ppm/°C resistor temperature coefficient, ±0.25% sampling resistor tolerance, ±10 mV and ±5 mV output voltage change due to load regulation and line regulation, respectively, and 1% reference accuracy.

Error due to temperature = 125°C × ±100 ppm/°C = ±1.25%

Error due to sampling resistor = ±0.25%

Error due to load regulation =
100% × (±0.01 V/3.3 V) = ±0.303%

Error due to line regulation =
100% × (±0.005 V/3.3 V) = ±0.152%

Error due to reference = ±1%

The worst-case error assumes that all errors vary in the same direction.

Worst-case error =
±(1.25% + 0.25% + 0.303% + 0.152% + 1%) = ±2.955%

Typical error assumes random variations, so a root square sum (rss) of the errors is used.

Typical error =
$\pm \sqrt{(1.25^2 + 0.25^2 + 0.303^2 + 0.152^2 + 1^2)} = \pm 1.655\%$

The LDO will never exceed the worst-case error, while the rss error is the most likely. The error distribution will center on the rss error and spread to include the worst-case error at the tails.

Load Transient Response

The load transient response is the output voltage variation for a load current step change. It is a function of the output capacitor value, the capacitor's equivalent series resistance (ESR), the gain-bandwidth of the LDO's control loop, and the size and slew rate of the load current change.

The slew rate of the load transient can have a dramatic effect on the load transient response. If the load transient is very slow, say 100 mA/µs, the control loop of the LDO may be able to follow the change. If, however, the load transient is faster than the loop can compensate, undesirable behavior such as excessive ringing due to low phase margin may occur.

Figure 8 shows the response of the ADM7172 to a 1 mA to 1.5 A load transient with a 3.75 A/µs slew rate. The 1.5 µs recovery time to 0.1% and minimal ringing indicate good phase margin.

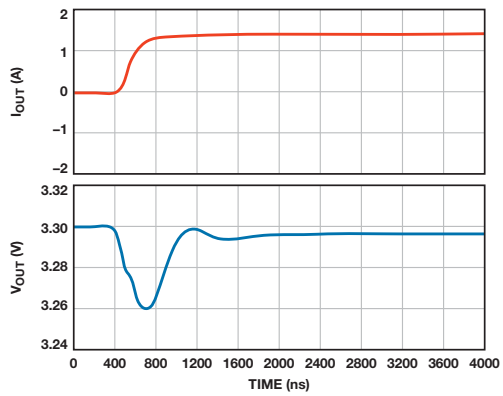

Figure 8. ADM7172 load transient response. 1 mA to 1.5 A load step in 400 ns (red). Output voltage (blue).

Line Transient Response

The line transient response is the output voltage variation for an input voltage step change. It is a function of the gain-bandwidth of the LDO's control loop, and the size and slew rate of the input voltage change.

Figure 9 shows the response of the ADM7150 to a 2-V input voltage step change. The output voltage deviation provides an indication of the loop bandwidth and the PSRR (see next section). The output voltage changes about 2 mV in response to a 2-V change in 1.5 µs, indicating a PSRR of about 60 dB at about 100 kHz.

Again, as in the case of load transients, the slew rate of the input voltage has a large effect on the apparent line transient response. A slowly changing input voltage, one well within the bandwidth of the LDO, can hide ringing or other undesirable behavior.

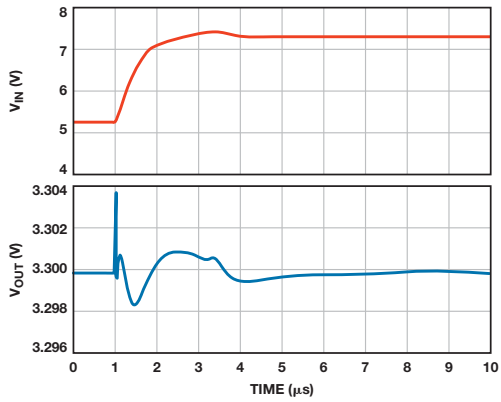

Figure 9. ADM7150 line transient response. 5 V to 7 V line step in 1.5 µs (red). Output voltage (blue).

Power Supply Rejection

Simply put, PSRR is a measure of how well a circuit suppresses extraneous signals (noise and ripple) on the power supply input to keep them from corrupting the output. PSRR is defined as

$$PSRR = 20 \times \log(VE_{IN}/VE_{OUT})$$

where VE_{IN} and VE_{OUT} are the extraneous signals appearing at the input and output, respectively.

For circuits such as ADCs, DACs, and amplifiers, PSRR applies to the inputs that supply power to the internal circuitry. With LDOs, the input power pin supplies power to the regulated output voltage as well as to the internal circuitry. PSRR has the same relation as dc line regulation, but includes the entire frequency spectrum.

Power supply rejection in the 100 kHz to 1 MHz range is very important, as switch-mode power supplies are frequently used in high-efficiency power systems, with LDOs cleaning up the noisy supply rails for the sensitive analog circuitry.

The LDO's control loop tends to be the dominant factor in determining power supply rejection. High value, low ESR capacitors can be beneficial, especially at frequencies beyond the gain-bandwidth of the control loop.

PSRR as a Function of Frequency

PSRR is not defined by a single value because it is frequency dependent. An LDO consists of a reference voltage, error amplifier, and a power-pass element, such as a MOSFET or bipolar transistor. The error amplifier provides dc gain to

regulate the output voltage. The ac gain of the error amplifier in large part determines the PSRR. A typical LDO can have as much as 80 dB of PSRR at 10 Hz, but the PSRR can fall to as little as 20 dB at a few tens of kilohertz.

Figure 10 shows the relationship between the error amplifier's gain-bandwidth and the PSRR. This simplified example ignores parasitics from the output capacitor and the pass element. The PSRR is the reciprocal of the open-loop gain until the gain starts to roll off at 3 kHz. The PSRR then decreases by 20 dB/decade until it reaches 0 dB at 3 MHz and up.

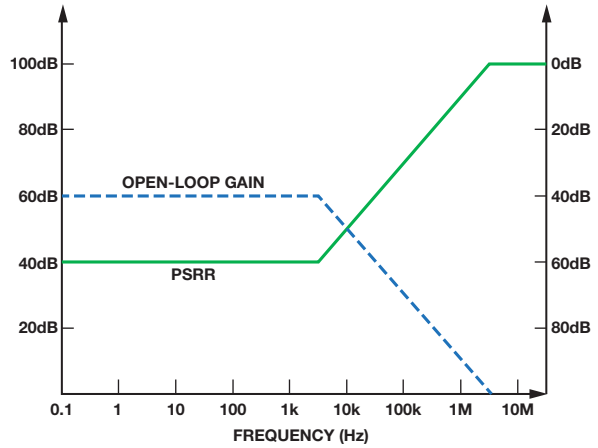

Figure 10. Simplified LDO gain vs. PSRR

Figure 11 shows three main frequency domains that characterize an LDO's PSRR: the reference PSRR region, the open-loop gain region, and the output capacitor region. The reference PSRR region is dependent on the PSRR of the reference amplifier and the LDO's open-loop gain. Ideally, the reference amplifier is fully isolated from perturbations in the power supply, but in practice, the reference need only reject power supply noise up to a few tens of hertz because the error amplifier feedback ensures high PSRR at low frequencies.

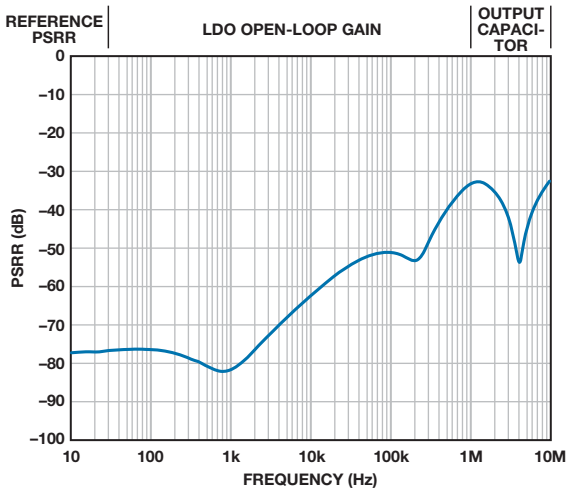

Figure 11. Typical LDO PSRR vs. frequency.

Above about 10 Hz, PSRR in the second region is dominated by the open-loop gain of the LDO. The PSRR in this region is a function of the error amplifier gain-bandwidth up to the unity gain frequency. At low frequencies, the ac gain of the error amplifier is equal to the dc gain. The gain remains constant until it reaches the 3-dB roll-off frequency. At frequencies above the 3-dB roll-off point, the ac gain of the error amplifier decreases with frequency, typically at 20 dB/decade.

Above the unity gain frequency of the error amplifier, the feedback of the control loop has no effect on the PSRR, which is determined by the output capacitor and any parasitics between the input and output voltages. The ESR and ESL of the output capacitor, as well as the board layout, strongly affect the PSRR at these frequencies. Careful attention to layout is essential to reduce the effect of any high-frequency resonances.

PSRR as a Function of Load Current

The load current affects the gain-bandwidth of the error amplifier feedback loop, so it also affects the PSRR. At light load currents, typically less than 50 mA, the output impedance of the pass element is high. The LDO's output appears to be an ideal current source due to the negative feedback of the control loop. The pole formed by the output capacitor and the pass element occurs at a relatively low frequency, so PSRR tends to increase at low frequencies. The high dc gain of the output stage at low currents also tends to increase the PSRR at frequencies well below the unity-gain point of the error amplifier.

At heavy load currents, the LDO output looks less like an ideal current source. The output impedance of the pass element decreases, lowering the gain of the output stage and reducing the PSRR between dc and the unity-gain frequency of the feedback loop. PSRR can fall dramatically as the load current rises, as shown in Figure 12. As the load increases from 400 mA to 800 mA, the PSRR of the ADM7150 decreases by 20 dB at 1 kHz.

The output stage bandwidth increases as the frequency of the output pole increases. At high frequencies, the PSSR should increase due to the increased bandwidth, but in practice, the high-frequency PSRR may not improve because of the decrease in overall loop gain. In general, PSRR at light loads is better than it is at heavy loads.

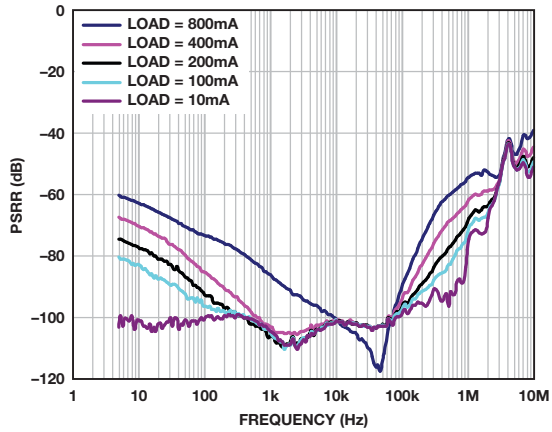

Figure 12. ADM7150 power supply rejection vs. frequency. V_{OUT} = 5 V, V_{IN} = 6.2 V.

PSRR as a Function of LDO Headroom

PSRR is also a function of the input-to-output voltage differential, or headroom. For a fixed headroom voltage, PSRR decreases as the load current increases; this is especially apparent at heavy load currents and small

headroom voltages. Figure 13 shows the difference in PSRR vs. headroom voltage for a 5-V ADM7172 with a 2-A load.

As the load current increases, the gain of the pass element (PMOSFET for the ADM7172) decreases as it leaves saturation and goes into the triode region of operation. This causes the overall loop gain of the LDO to decrease, resulting in a lower PSRR. The smaller the headroom voltage, the more dramatic the reduction in gain. At small headroom voltages, the control loop has no gain at all, and the PSRR falls to nearly zero.

Another factor that reduces the loop gain is nonzero resistance of the pass element, RDS_{ON}. The voltage drop across RDS_{ON} due to the load current subtracts from the headroom of the active portion of the pass element. For example, with a 1-Ω pass element, a 200-mA load current reduces the headroom by 200 mV. When operating LDOs at headroom voltages of 1 V or less, this voltage drop must be accounted for when estimating the PSRR.

In dropout, the PSRR is due to the pole formed by RDS_{ON} and the output capacitor. At a very high frequency, the PSRR will be limited by the ratio of the output capacitor ESR to RDS_{ON}.

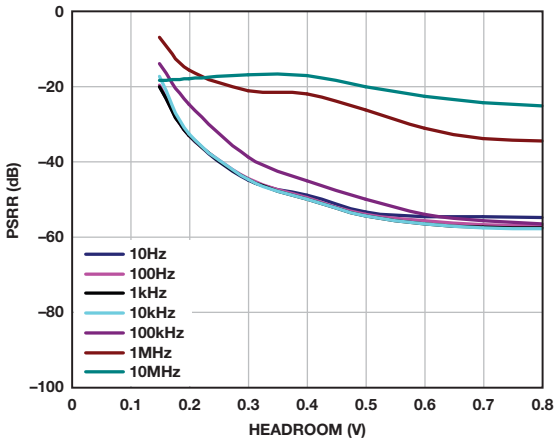

Figure 13. ADM7172 power supply rejection vs. headroom, V_{OUT} = 5 V, 2 A load current.

Comparing LDO PSRR Specifications

When comparing LDO PSRR specifications, make sure that the measurements are made under the same test conditions. Many older LDOs specify PSRR at only 120 Hz or 1 kHz with no mention of headroom voltage or load current. At the least, PSRR in the electrical specification table should be listed for different frequencies. Ideally, typical characteristic plots of PSRR under different load and headroom voltages should be used to make meaningful comparisons.

The output capacitor also affects the LDO PSRR at high frequency. For example, a 1-µF capacitor has 10× the impedance of a 10-µF capacitor. The capacitor value is especially important at frequencies above the error amplifier's unity-gain crossover frequency, where the attenuation of power supply noise is a function of the output capacitance. When comparing PSRR figures, the output capacitor must be the same type and value for the comparison to be valid.

Output Noise Voltage

Output noise voltage is the rms output noise voltage over a given range of frequencies (typically 10 Hz or 100 Hz to 100 kHz) under the conditions of a constant output current and a ripple-free input voltage. The major sources of output noise in LDOs are the internal reference voltage and the error amplifier. Modern LDOs operate with internal bias currents of just a few tens of nanoamps in order to achieve quiescent currents of 15 µA or less. These low bias currents require the use of bias resistors of up to a GΩ. Output noise typically ranges from 5 µV rms to 100 µV rms. Figure 14 shows the output noise vs. load current for the ADM7172.

Some LDOs, such as the ADM7172, can use an external resistor divider to set the output voltage above the initial set point, allowing a 1.2-V device to provide a 3.6-V output, for example. A noise reduction network can be added to this divider to return the output noise to a level close to that of the original fixed voltage version.

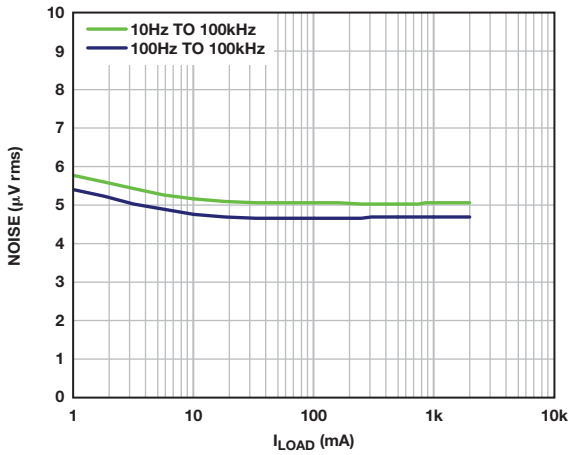

Figure 14. ADM7172 output noise vs. load current.

Another way to express the output noise of an LDO is the noise spectral density. The rms noise over a 1-Hz bandwidth at a given frequency is plotted over a wide frequency range. This information can then be used to compute the rms noise at a particular frequency for a given bandwidth. Figure 15 shows the noise spectral density from 1 Hz to 10 MHz for the ADM7172.

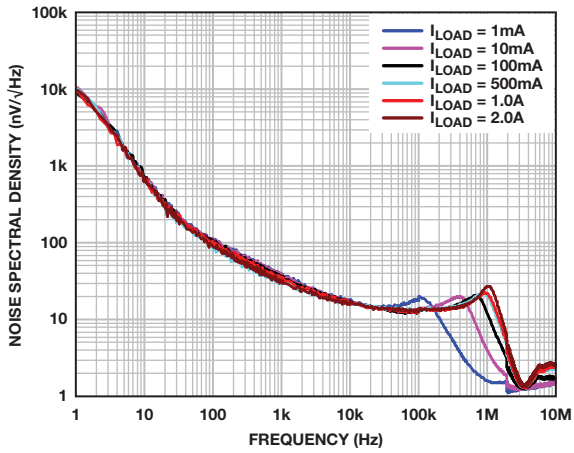

Figure 15. ADM7172 noise spectral density vs. load current.

Conclusion

LDOs are outwardly simple devices that provide a critical function. Many factors must be considered to apply them correctly and achieve optimal results. With a basic understanding of commonly used LDO terms, the design engineer can successfully navigate the data sheet to determine parameters that are most important for the design.

References

Linear Regulators

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