Phase-Locked Loops for High-Frequency Receivers and Transmitters–Part 2

by Mike Curtin and Paul O'Brien

The *first part* of this series of articles introduced the basic concepts of *phase-locked loops* (PLLs). The PLL architecture and principle of operation was described and accompanied by an example of where a PLL might be used in a communication system.

In this second part, we will focus on a detailed examination of two critical specifications associated with PLLs: *phase noise* and *reference spurs*. What causes them and how can they be minimized? The discussion will include measurement techniques and the effect of these errors on system performance. We will also consider *output leakage current*, with an example showing its significance in open-loop modulation schemes.

Noise in Oscillator Systems

In any oscillator design, frequency stability is of critical importance. We are interested in both long-term and short-term stability. *Long-term* frequency stability is concerned with how the output signal varies over a long period of time (hours, days or months). It is usually specified as the ratio, $\Delta f/f$ for a given period of time, expressed as a percentage or in dB.

Short-term stability, on the other hand, is concerned with variations that occur over a period of seconds or less. These variations can be random or periodic. A spectrum analyzer can be used to examine the short-term stability of a signal. Figure 1 shows a typical spectrum, with random and discrete frequency components causing a broad skirt and spurious peaks.

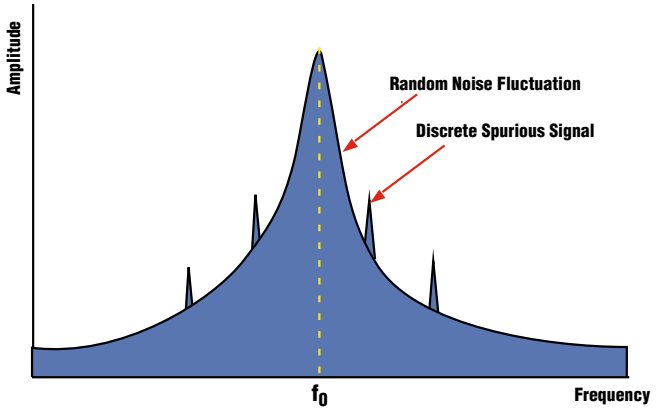

Figure 1. Short-term stability in oscillators.

The discrete spurious components could be caused by known clock frequencies in the signal source, power line interference, and mixer products. The broadening caused by random noise fluctuation is due to *phase noise*. It can be the result of thermal noise, shot noise and/or flicker noise in active and passive devices.

Phase Noise in Voltage-Controlled Oscillators

Before we look at phase noise in a PLL system, it is worth considering the phase noise in a *voltage-controlled oscillator* (VCO). An ideal VCO would have no phase noise. Its output as seen on a spectrum analyzer would be a single spectral line. In practice, of course, this is not the case. There will be jitter on the output, and a spectrum analyzer would show phase noise. To help understand phase noise, consider a phasor representation, such as that shown in Figure 2.

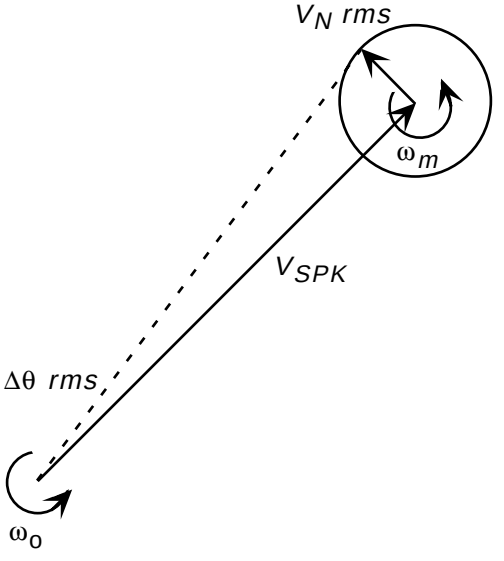

Figure 2. Phasor representation of phase noise.

A signal of angular velocity ω_O and peak amplitude V_{SPK} is shown. Superimposed on this is an error signal of angular velocity ω_m. $\Delta\theta$rms represents the rms value of the phase fluctuations and is expressed in rms degrees.

In many radio systems, an overall integrated phase error specification must be met. This overall phase error is made up of the PLL phase error, the modulator phase error and the phase error due to base band components. In GSM, for example, the total allowed is 5 degrees rms.

Leeson's Equation

Leeson (see Reference 6) developed an equation to describe the different noise components in a VCO.

$$L_{PM} \approx 10\log\left[\frac{FkT}{A}\frac{1}{8Q_L^2}\left(\frac{f_O}{f_m}\right)^2\right] \quad (1)$$

where:

L_{PM} is single-sideband phase noise density (dBc/Hz)
F is the device noise factor at operating power level A (linear)
k is Boltzmann's constant, 1.38×10^{-23} J/K
T is temperature (K)
A is oscillator output power (W)
Q_L is loaded Q (dimensionless)
f_O is the oscillator carrier frequency
f_m is the frequency offset from the carrier

For Leeson's equation to be valid, the following must be true:

- f_m, the offset frequency from the carrier, is greater than the 1/f flicker corner frequency;
- the noise factor at the operating power level is known;
- the device operation is linear;
- Q includes the effects of component losses, device loading and buffer loading;
- a single resonator is used in the oscillator.

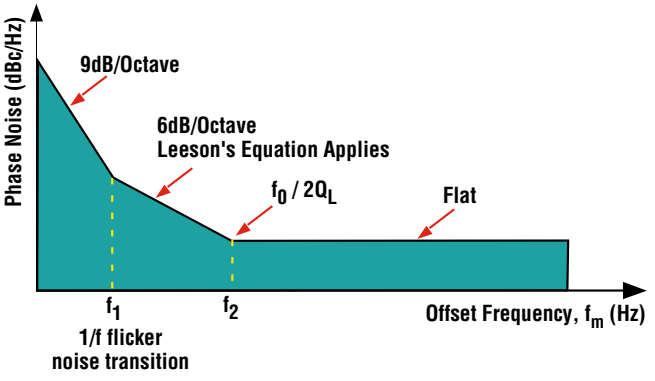

Figure 3. Phase noise in a VCO vs. frequency offset.

Leeson's equation only applies in the knee region between the break (f_1) to the transition from the "1/f" (more generally 1/f$^\gamma$) flicker noise frequency to a frequency beyond which amplified white noise dominates (f_2). This is shown in Figure 3 [γ = 3]. f_1 should be as low as possible; typically, it is less than 1 kHz, while f_2 is in the region of a few MHz. High-performance oscillators require devices specially selected for low 1/f transition frequency. Some guidelines to minimizing the phase noise in VCOs are:

1. Keep the tuning voltage of the varactor sufficiently high (typically between 3 and 3.8 V)
2. Use filtering on the dc voltage supply.
3. Keep the inductor Q as high as possible. Typical off-the-shelf coils provide a Q of between 50 and 60.
4. Choose an active device that has minimal noise figure as well as low flicker frequency. The flicker noise can be reduced by the use of feedback elements.
5. Most active device exhibit a broad U-shaped noise-figure-vs.-bias-current curve. Use this information to choose the optimal operating bias current for the device.
6. Maximize the average power at the tank circuit output.
7. When buffering the VCO, use devices with the lowest possible noise figure.

Closing The Loop

Having looked at phase noise in a free-running VCO and considered how it can be minimized, we will now consider the effect of closing the loop (see *Part 1* of the series) on phase noise.

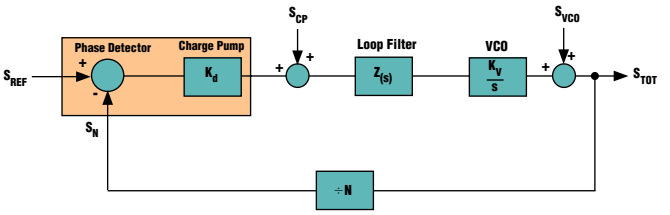

Figure 4. PLL-phase-noise contributors.

Figure 4 shows the main phase noise contributors in a PLL. The system transfer function may be described by the following equations.

$$Closed\ Loop\ Gain = \frac{G}{1 + GH} \tag{2}$$

$$G = \frac{K_d \times K_v \times Z(s)}{s} \tag{3}$$

$$H = \frac{1}{N} \tag{4}$$

$$Closed\ Loop\ Gain = \frac{\frac{K_d \times K_v \times Z(s)}{s}}{\frac{K_d \times K_v \times Z(s)}{N \times s}} \tag{5}$$

For the discussion that follows, we will define S_{REF} as the noise that appears on the reference input to the phase detector. It is dependent on the reference divider circuitry and the spectral purity of the main reference signal. S_N is the noise due to the feedback divider appearing at the frequency input to the phase detector. S_{CP} is the noise due to the phase detector (depending on its implementation). And S_{VCO} is the phase noise of the VCO as described by equations developed earlier.

The overall phase noise performance at the output depends on the terms described above. All the effects at the output are added in an rms fashion to give the total noise of the system. Thus:

$$S_{TOT}{}^2 = X^2 + Y^2 + Z^2 \tag{6}$$

where:

$S_{TOT}{}^2$ is the total phase noise power at the output

X^2 is the noise power at the output due to S_N and S_{REF}.

Y^2 is the noise power at the output due to S_{CP}.

Z^2 is the noise power at the output due to S_{VCO}.

The noise terms at the PD inputs, S_{REF} and S_N, will be operated on in the same fashion as F_{REF} and will be multiplied by the closed loop gain of the system.

$$X^2 = \left(S_{REF}{}^2 + S_N{}^2\right) \times \left(\frac{G}{1 + GH}\right)^2 \tag{7}$$

At low frequencies, inside the loop bandwidth,

$$GH >> 1\ and\ X^2 = \left(S_{REF}{}^2 + S_N{}^2\right) \times N^2 \tag{8}$$

At high frequencies, outside the loop bandwidth,

$$G << 1 \; and \; X^2 \Rightarrow 0 \tag{9}$$

The overall output noise contribution due to the phase detector noise, S_{CP}, can be calculated by referencing S_{CP} back to the input of the PFD. The equivalent noise at the PD input is S_{CP}/K_d. This is then multiplied by the closed-loop gain:

$$Y^2 = {S_{CP}}^2 \times \left(\frac{1}{K_d}\right)^2 \times \left(\frac{G}{1+GH}\right)^2 \tag{10}$$

Finally, the contribution of the VCO noise, S_{VCO}, to the output phase noise is calculated in a similar manner. The forward gain this time is simply 1. Therefore its contribution to the output noise is:

$$Z^2 = {S_{VCO}}^2 \times \left(\frac{1}{1+GH}\right)^2 \tag{11}$$

G, the forward loop gain of the closed loop response, is usually a low pass function; it is very large at low frequencies and small at high frequencies. H is a constant, 1/N. The denominator of the above expression is therefore low pass, so S_{VCO} is actually high-pass filtered by the closed loop.

A similar description of the noise contributors in a PLL/VCO can be found in Reference 1. Recall that the closed-loop response is a low-pass filter with a 3-dB cutoff frequency, B_W, denoted the *loop bandwidth*. For frequency offsets at the output less than B_W, the dominant terms in the output phase noise response are X and Y, the noise terms due to reference noise, N (counter noise), and charge pump noise. Keeping S_N and S_{REF} to a minimum, keeping K_d large and keeping N small will thus minimize the phase noise inside the loop bandwidth, B_W. Because N programs the output frequency, it is not generally available as a factor in noise reduction.

For frequency offsets much greater than B_W, the dominant noise term is that due to the VCO, S_{VCO}. This is due to the high pass filtering of the VCO phase noise by the loop. A small value of B_W would be desirable as it would minimize the total integrated output noise (phase error). However a small B_W results in a slow transient response and increased contribution from the VCO phase noise inside the loop bandwidth. The loop bandwidth calculation therefore must trade off transient response and total output integrated phase noise.

To show the effect of closing the loop on a PLL, Figure 5 shows an overlay of the output of a free-running VCO and the output of a VCO as part of a PLL. Note that the in-band noise of the PLL has been attenuated compared to that of the free-running VCO.

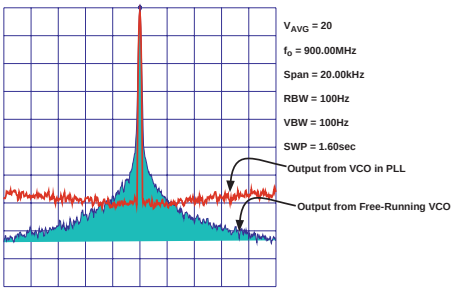

Figure 5. Phase noise on a free-running VCO and a PLL-connected VCO.

Phase Noise Measurement

One of the most common ways of measuring phase noise is with a high frequency spectrum analyzer. Figure 6 is a typical example of what would be seen.

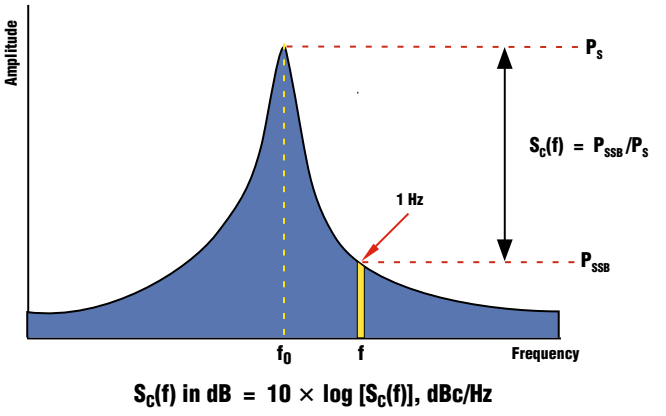

Figure 6. Phase noise definition.

With the spectrum analyzer we can measure the spectral density of phase fluctuations per unit bandwidth. VCO phase noise is best described in the frequency domain where the spectral density is characterized by measuring the noise sidebands on either side of the output signal center frequency. Phase noise power is specified in decibels relative to the carrier (dBc/Hz) at a given frequency offset from the carrier. The following equation describes this SSB phase noise (dBc/Hz).

$$S_C(f) = 10 \log \frac{P_S}{P_{SSB}} \tag{12}$$

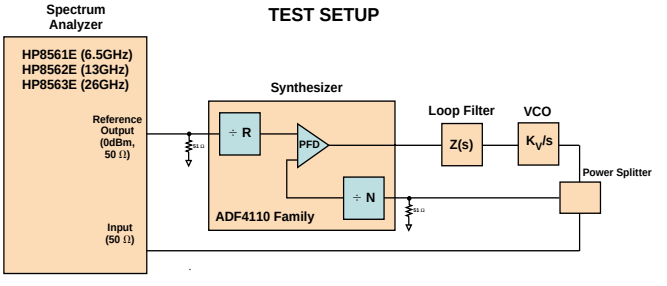

Figure 7. Measuring phase noise with a spectrum analyzer.

The 10-MHz, 0-dBm reference oscillator, available on the spectrum analyzer's rear-panel connector, has excellent phase noise performance. The R divider, N divider, and the phase detector are part of ADF4112 frequency synthesizer. These dividers are programmed serially under the control of a PC. The frequency and phase noise performance are observed on the spectrum analyzer.

Figure 8 illustrates a typical phase noise plot of a PLL synthesizer using an ADF4112 PLL with a Murata VCO, MQE520-1880. The frequency and phase noise were measured in a 5-kHz span. The reference frequency used was f_{REF} = 200 kHz (R = 50) and the output frequency was 1880 MHz (N = 9400). If this were an ideal-world PLL synthesizer, a single discrete tone would be displayed rising up above the spectrum analyzer's noise floor. What is displayed here is the tone, with the phase noise due to the loop components. The loop filter values were chosen to give a loop

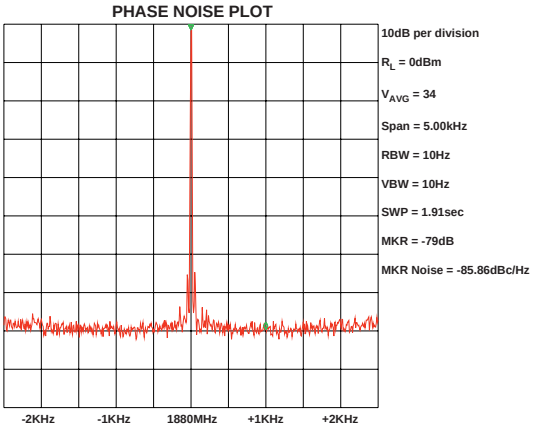

Figure 8. Typical spectrum-analyzer output.

bandwidth of approximately 20 kHz. The flat part of the phase noise for frequency offsets less than the loop bandwidth is actually the phase noise as described by X^2 and Y^2 in the section "closing the loop" for cases where f is inside the loop bandwidth. It is specified at a 1-kHz offset. The value measured, the phase-noise power in a 1-Hz bandwidth, was –85.86 dBc/Hz. It is made up of the following:

1. Relative power in dBc between the carrier and the sideband noise at 1-kHz offset.
2. The spectrum analyzer displays the power for a certain resolution bandwidth (RBW). In the plot, a 10-Hz RBW is used. To represent this power in a 1-Hz bandwidth, 10log(RBW) must be subtracted from the value obtained from (1).
3. A correction factor, which takes into account the implementation of the RBW, the log display mode and detector characteristic, must be added to the result obtained in (2).
4. Phase noise measurement with the HP 8561E can be made quickly by using the marker noise function, MKR NOISE. This function takes into account the above three factors and displays the phase noise in dBc/Hz.

The phase noise measurement above is the total output phase noise at the VCO output. If we want to estimate the contribution of the PLL device (noise due to phase detector, R&N dividers and the phase detector gain constant), the result must be divided by N^2 (or $20 \times \log N$ be subtracted from the above result). This gives a phase-noise floor of $[-85.86 - 20 \times \log(9400)] = -165.3$ dBc/Hz.

Reference Spurs

In an integer-N PLL (where the output frequency is an integer multiple of the reference input), reference spurs are caused by the fact that the charge pump output is being continuously updated at the reference frequency rate. Consider

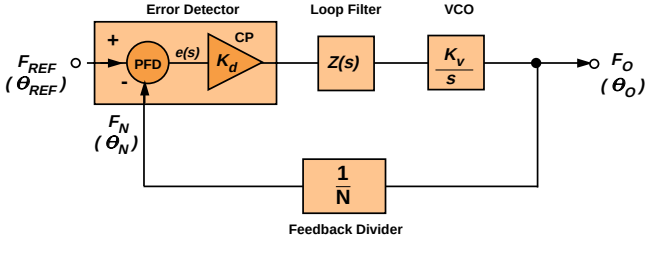

Figure 9. Basic PLL model.

again the basic model for the PLL which was discussed in Part 1 of this series. This is shown again in Figure 9.

When the PLL is in lock, the phase and frequency inputs to the PFD (f_{REF} and f_N) are essentially equal, and, in theory, one would expect that there to be no output from the PFD. However, this can create problems (to be discussed in Part 3 of this series), so the PFD is designed such that, in the locked condition, the current pulses from the charge pump will typically be as shown in Figure 10.

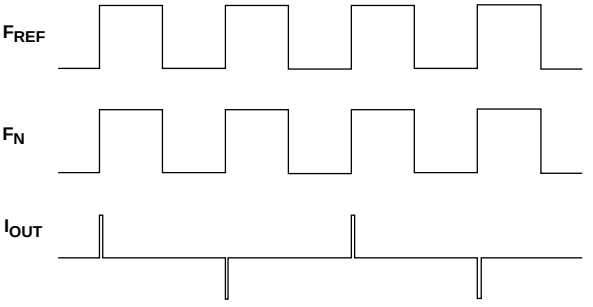

Figure 10. Output current pulses from the PFD charge pump.

Although these pulses have a very narrow width, the fact that they exist means that the dc voltage driving the VCO is modulated by a signal of frequency f_{REF}. This produces *reference spurs* in the RF output occurring at offset frequencies that are integer multiples of f_{REF}. A spectrum analyzer can be used to detect reference spurs. Simply increase the span to greater than twice the reference frequency. A typical plot is shown in Figure 11. In this case the reference frequency is 200 kHz and the diagram clearly shows reference spurs at ±200 kHz from the RF output of 1880 MHz. The level of these spurs is –90 dB. If the span were increased to more than four times the reference frequency, we would also see the spurs at $(2 \times f_{REF})$.

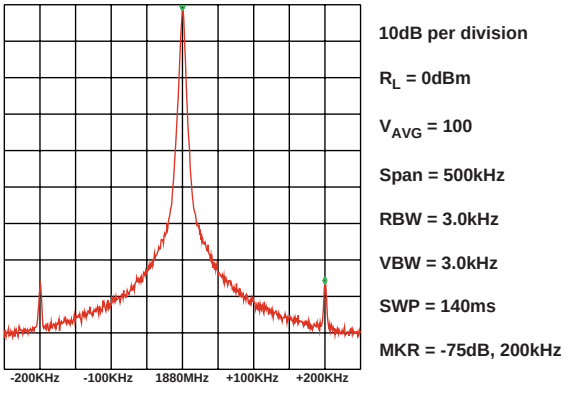

Figure 11. Output spectrum showing reference spurs.

Charge Pump Leakage Current

When the CP output from the synthesizer is programmed to the high impedance state, there should, in theory, be no leakage current flowing. In practice, in some applications the level of leakage current will have an impact on overall system performance. For example, consider an application where a PLL is used in open-loop mode for frequency modulation—a simple and inexpensive way of implementing FM that also allows higher data rates than modulating in closed-loop mode. For FM, a closed-loop method works fine but the data rate is limited by the loop bandwidth.

A system that uses open-loop modulation is the European cordless telephone system, DECT. The output carrier frequencies are in a range of 1.77 GHz to 1.90 GHz and the data rate is high; 1.152 Mbps.

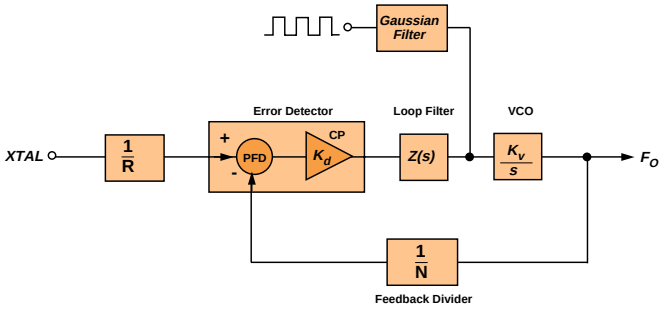

Figure 12. Block diagram of open-loop modulation.

A block diagram of open-loop modulation is shown in Figure 12. The principle of operation is as follows: The loop is initially closed to lock the RF output, $f_{OUT} = N f_{REF}$. The modulating signal is turned on and at first the modulation signal is simply the dc mean of the modulation. The loop is then opened, by putting the CP output of the synthesizer into high-impedance mode, and the modulation data is fed to the Gaussian filter. The modulating voltage then appears at the VCO where it is multiplied by K_V. When the data burst finishes, the loop is returned to the closed loop mode of operation.

As the VCO usually has a high sensitivity (typical figures are between 20 and 80 MHz/volt), any small voltage drift before the VCO will cause the output carrier frequency to drift. This voltage drift, and hence the system frequency drift, is directly dependent on the leakage current of the charge pump, CP, when in the high impedance state. This leakage will cause the loop capacitor to charge or discharge depending on the polarity of the leakage current. For example, a leakage current of 1 nA would cause the voltage on the loop capacitor (1000 pF for example) to charge or discharge by dV/dt = I/C (1 V/s in this case). This, in turn, would cause the VCO to drift. So, if the loop is open for 1 ms and the K_V of the VCO is 50 MHz/Volt, the frequency drift caused by 1-nA leakage into a 1000-pF loop capacitor would be 50 kHz. In fact, the DECT bursts are generally shorter (0.5 ms), so the drift will be even less in practice for the loop capacitance and leakage current used in the example. However, it does serve to illustrate the importance of charge-pump leakage in this type of application.

Receiver Sensitivity

Receiver sensitivity specifies the ability of the receiver to respond to a weak signal. Digital receivers use maximum bit-error rate (BER) at a certain rf level to specify performance. In general, device gains, noise figures, image noise, and local-oscillator (LO) wideband noise all combine to produce an equivalent noise figure. This is then used to calculate the overall receiver sensitivity.

Wideband noise in the LO can elevate the IF noise level and thus degrade the overall noise factor. For example, wideband phase noise at $F_{LO} + F_{IF}$ will produce noise products at F_{IF}. This directly impacts the receiver sensitivity. This wideband phase noise is primarily dependent on the VCO phase noise.

Close-in phase noise in the LO will also impact sensitivity. Obviously, any noise close to F_{LO} will produce noise products close to F_{IF} and impact sensitivity directly.

Receiver Selectivity

Receiver selectivity specifies the tendency of a receiver to respond to channels adjacent to the desired reception channel. *Adjacent-channel interference* (ACI), a commonly used term in wireless systems, is also used to describe this phenomenon. When considering the LO section, the reference spurs are of particular importance with regard to selectivity. Figure 13 is an attempt to illustrate how a spurious signal at the LO, having the same spacing as the channel-spacing frequency, can translate energy from an adjacent radio channel directly onto the IF. This is of particular concern if the desired received signal is distant and weak and the unwanted adjacent channel is nearby and strong, which can often be the case. So, the lower the reference spurs in the PLL, the better it will be for system selectivity.

Conclusion

In Part 2 of this series we have discussed some of the critical specifications associated with PLL synthesizers, described measurement techniques, and shown examples of results. In addition, there has been a brief discussion of the system implications of phase noise, reference spurs and leakage current.

In the final part of this series, we will examine the building blocks that go to make up a PLL synthesizer. In addition, there will be a comparison between integer-N and fractional-N architectures for PLL.

Acknowledgment

The authors would like to acknowledge Brendan Daly of the Analog Devices GP RF Applications Group in Limerick for the plots of phase noise and reference spurs.

References

1. Mini-Circuits Corporation, *VCO Designers' Handbook*, 1996.
2. L.W. Couch, *Digital and Analog Communications Systems*, Macmillan Publishing Company, New York, 1990.
3. P. Vizmuller, *RF Design Guide*, Artech House, 1995.
4. R.L. Best, *Phase Locked Loops: Design, Simulation and Applications*, 3rd edition, McGraw-Hill, 1997.
5. D.E. Fague, "Open Loop Modulation of VCOs for Cordless Telecommunications," *RF Design*, July 1994.
6. D. B. Leeson, "A Simplified Model of Feedback Oscillator Noise Spectrum," *Proceedings of the IEEE*, Volume 42, February 1965, pp. 329–330.

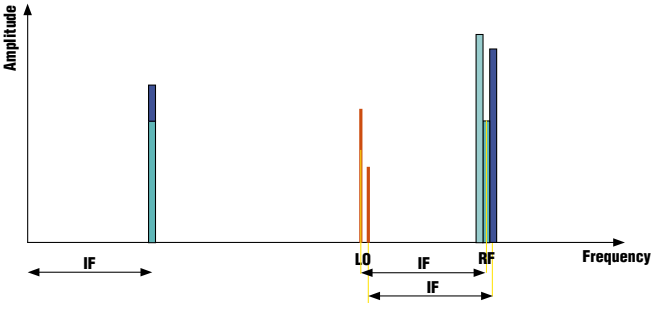

Figure 13. Adjacent Channel Interference.