Phase-Locked Loops for High-Frequency Receivers and Transmitters–Part 1

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This 3-part series of articles is intended to give a comprehensive overview of the use of PLLs (phase-locked loops) in both wired and wireless communication systems.

In this first part, the emphasis is on the introductory concepts of PLLs. The basic PLL architecture and principle of operation is described. We will also give an example of where PLLs are used in communication systems. We will finish the first installment by showing a practical PLL circuit using the ADF4111 Frequency Synthesizer and the VCO190-902T Voltage-Controlled Oscillator.

In the second part, we will examine in detail the critical specifications associated with PLLs: phase noise, reference spurs and output leakage current. What causes these and how can they be minimized? What effect do they have on system performance?

The final installment will contain a detailed description of the blocks that go to make up a PLL synthesizer and the architecture of an Analog Devices synthesizer. There will also be a summary of synthesizers and VCOs currently available on the market, with a list of ADI's current offerings.

PLL BASICS

A phase-locked loop is a feedback system combining a voltage-controlled oscillator and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. Phase-locked loops can be used, for example, to generate stable output frequency signals from a fixed low-frequency signal. The first phase-locked loops were implemented in the early 1930s by a French engineer, de Bellescize. However, they only found broad acceptance in the marketplace when integrated PLLs became available as relatively low-cost components in the mid-1960s.

The phase locked loop can be analyzed in general as a negative-feedback system with a forward gain term and a feedback term.

A simple block diagram of a voltage-based negative-feedback system is shown in Figure 1.

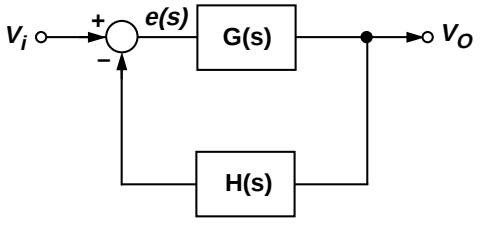

Figure 1. Standard negative-feedback control system model.

In a phase-locked loop, the error signal from the phase comparator is proportional to the relative phase of the input and feedback signals. The average output of the phase detector will be constant when the input and feedback signals are the same frequency. The usual equations for a negative-feedback system apply.

$$Forward\ Gain = G(s),\ [s = j\omega = j2\pi f]$$

$$Loop\ Gain = G(s) \times H(s)$$

$$Closed\text{-}Loop\ Gain = \frac{G(s)}{1 + G(s)H(s)}$$

Because of the integration in the loop, at low frequencies the steady state gain, $G(s)$, is high and

$$V_O/V_I,\ Closed\text{-}Loop\ Gain = \frac{1}{H}$$

The components of a PLL that contribute to the loop gain include:

1. The *phase detector* (PD) and *charge pump* (CP).
2. The *loop filter*, with a transfer function of $Z(s)$
3. The *voltage-controlled oscillator* (VCO), with a sensitivity of K_V/s
4. The *feedback divider*, $1/N$

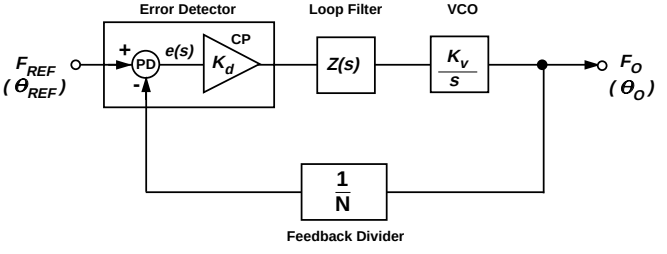

Figure 2. Basic phase-locked-loop model.

If a linear element like a four-quadrant multiplier is used as the phase detector, and the loop filter and VCO are also analog elements, this is called an analog, or *linear PLL* (LPLL).

If a *digital* phase detector (EXOR gate or J-K flip flop) is used, and everything else stays the same, the system is called *a digital PLL* (DPLL).

If the PLL is built exclusively from digital blocks, without any passive components or linear elements, it becomes an *all-digital PLL* (ADPLL).

Finally, with information in digital form, and the availability of sufficiently fast processing, it is also possible to develop PLLs in the software domain. The PLL function is performed by software and runs on a DSP. This is called a *software PLL* (SPLL).

Referring to Figure 2, a system for using a PLL to generate higher frequencies than the input, the VCO oscillates at an angular frequency of ω_O. A portion of this signal is fed back to the error detector, via a frequency divider with a ratio 1/N. This divided-down frequency is fed to one input of the error detector. The other input in this example is a fixed reference signal. The error detector compares the signals at both inputs. When the two signal inputs are equal in frequency, the error will be constant and the loop is said to be in a "locked" condition. If we simply look at the error signal, the following equations may be developed.

$$e(s) = \Phi_{REF} - \frac{\Phi_O}{N}$$

$$\frac{de(s)}{dt} = F_{REF} - \frac{F_O}{N}$$

When

$$e(s) = constant, \frac{F_O}{N} = F_{REF}$$

Thus

$$F_O = N\ F_{REF}$$

In commercial PLLs, the phase detector and charge pump together form the error detector block. When $F_O \neq N F_{REF}$, the error detector will output source/sink current pulses to the low-pass loop filter. This smooths the current pulses into a voltage which in turn drives the VCO. The VCO frequency will then increase or decrease as necessary, by K_V DV, where K_V is the VCO sensitivity in MHz/Volt and DV is the change in VCO input voltage. This will continue until $e(s)$ is zero and the loop is locked. The charge pump and VCO thus serves as an integrator, seeking to increase or decrease its output frequency to the value required so as to restore its input (from the phase detector) to zero.

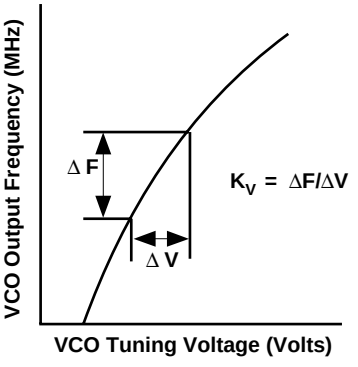

Figure 3. VCO transfer function.

The overall transfer function (CLG or Closed-Loop Gain) of the PLL can be expressed simply by using the CLG expression for a negative feedback system as given above.

$$\frac{F_O}{F_{REF}} = \frac{Forward\ Gain}{1 + Loop\ Gain}$$

$$Forward\ Gain, G = \frac{K_D\ K_V\ Z(s)}{s}$$

$$Loop\ Gain, GH = \frac{K_D\ K_V\ Z(s)}{Ns}$$

When GH is much greater than 1, we can say that the closed loop transfer function for the PLL system is N and so

$$F_{OUT} = N \times F_{REF}$$

The loop filter is a low-pass type, typically with one pole and one zero. The transient response of the loop depends on:

1. the magnitude of the pole/zero,
2. the charge pump magnitude,
3. the VCO sensitivity,
4. the feedback factor, N.

All of the above must be taken into account when designing the loop filter. In addition, the filter must be designed to be stable (usually a phase margin of $\pi/4$ is recommended). The 3-dB cutoff frequency of the response is usually called the loop bandwidth, B_W. Large loop bandwidths result in very fast transient response. However, this is not always advantageous, as we shall see in Part 2, since there is a tradeoff between fast transient response and reference spur attenuation.

PLL APPLICATIONS TO FREQUENCY UPSCALING

The phase-locked loop allows stable high frequencies to be generated from a low-frequency reference. Any system that requires stable high frequency tuning can benefit from the PLL technique. Examples of these applications include wireless base stations, wireless handsets, pagers, CATV systems, clock-recovery and -generation systems. A good example of a PLL application is a GSM handset or base station. Figure 4 shows the receive section of a GSM base station.

In the GSM system, there are 124 channels (8 users per channel) of 200-kHz width in the RF band. The total bandwidth occupied is 24.8 MHz, which must be scanned for activity. The handset has a transmit (Tx) range of 880 MHz to 915 MHz and a receive (Rx) range of 925 MHz to 960 MHz. Conversely, the base station has a Tx range of 925 MHz to 960 MHz and an Rx range of 880 MHz to 915 MHz. For this example, we will consider just the base station transmit and receive sections. The frequency bands for GSM900 and DCS1800 Base Station Systems are shown in Table 1. Table 2 shows the channel numbers for the carrier frequencies (RF channels) within the frequency bands of Table 1. $Fl(n)$ is the center frequency of the RF channel in the lower band (Rx) and $Fu(n)$ is the corresponding frequency in the upper band (Tx).

Table 1. Frequency Bands for GSM900 and DCS1800 Base Station Systems

	T_X	R_X
P-GSM900	935 to 960 MHz	890 to 915 MHz
DCS1800	1805 to 1880 MHz	1710 to 1785 MHz
E-GSM900	925 to 960 MHz	880 to 915 MHz

Table 2. Channel Numbering for GSM900 and DCS1800 Base Station Systems

	R_X		T_X
PGSM900	Fl(n) = 890 + 0.2 × (n)	1 ≤ n ≤ 124	Fu(n) = Fl(n) + 45
EGSM900	Fl(n) = 890 + 0.2 × (n) Fl(n) = 890 + 0.2 × (n – 1024)	0 ≤ n ≤ 124 975 ≤ n ≤ 1023	Fu(n) = Fl(n) + 45
DCS1800	Fl(n) = 1710.2 + 0.2 × (n – 512)	512 ≤ n ≤ 885	Fu(n) = Fl(n) + 95

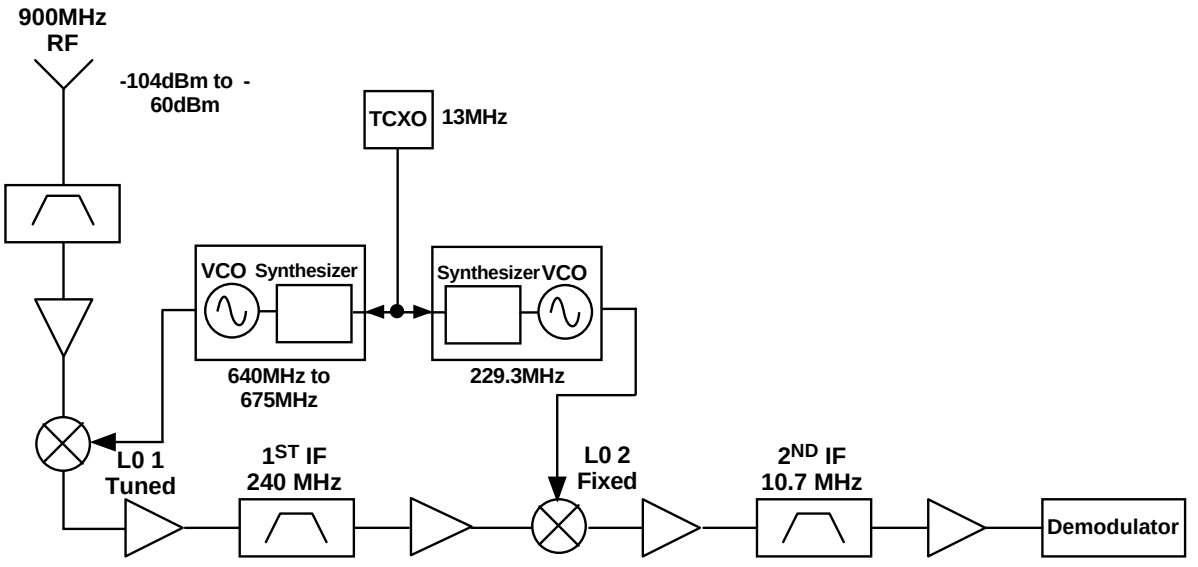

Figure 4. Signal chain for GMS base-station receiver.

The 900-MHz RF input is filtered, amplified and applied to the first stage mixer. The other mixer input is driven from a tuned local oscillator (LO). This must scan the input frequency range to search for activity on any of the channels. The actual implementation of the LO is by means of the PLL technique already described. If the 1st intermediate-frequency (IF) stage is centered at 240 MHz, then the LO must have a range of 640 MHz to 675 MHz in order to cover the RF input band. When a 200-kHz reference frequency is chosen, it will be possible to sequence the VCO output through the full frequency range in steps of 200 kHz. For example, when an output frequency of 650 MHz is desired, N will have a value of 3250. This 650-MHz LO will effectively check the 890-MHz RF channel ($F_{RF} - F_{LO} = F_{IF}$ or $F_{RF} = F_{LO} + F_{IF}$). When N is incremented to 3251, the LO frequency will now be 650.2 MHz and the RF channel checked will be 890.2 MHz. This is shown graphically in Figure 5.

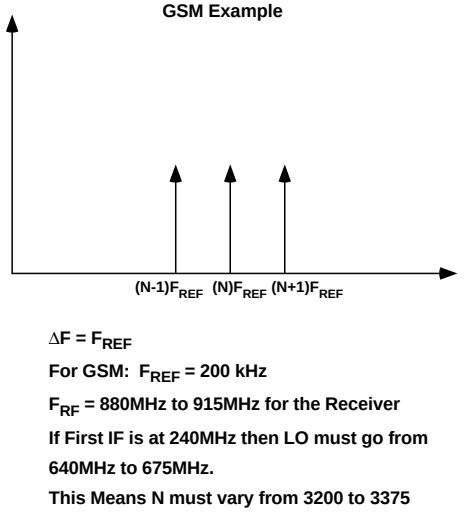

Figure 5. Testing frequencies for GSM base-station receiver.

It is worth noting that, in addition to the tunable RF LO, the receiver section also uses a fixed IF (in the example shown this is 240 MHz). Even though frequency tuning is not needed on this IF, the PLL technique is still used. The reason for this is that it is an affordable way of using the stable system reference frequency to produce the high frequency IF signal. Several synthesizer manufacturers recognize this fact by offering dual versions of the devices: one operating at the high RF frequency (>800 MHz) and one operating at the lower IF frequency (500 MHz or less).

On the transmit side of the GSM system, similar requirements exist. However, it is more common to go directly from baseband to the final RF in the Transmit section; this means that the typical T_X VCO for a base station has a range of 925 MHz to 960 MHz (RF band for the Transmit section).

CIRCUIT EXAMPLE

Figure 6 shows an actual implementation of the local oscillator for the transmit section of a GSM handset. We are assuming direct baseband to RF up-conversion. This circuit uses the new ADF4111 PLL Frequency Synthesizer from ADI and the VCO190-902T Voltage Controlled Oscillator from Vari-L Corporation (http://www.vari-L.com/).

The reference input signal is applied to the circuit at $FREF_{IN}$ and is terminated in 50 Ω. This reference input frequency is typically 13 MHz in a GSM system. In order to have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference divider of the ADF4111.

The ADF4111 is an integer-N PLL frequency synthesizer, capable of operating up to an RF frequency of 1.2 GHz. In this integer-N type of synthesizer, N can be programmed from 96 to 262,000 in discrete integer steps. In the case of the handset transmitter, where an output range of 880 MHz to 915 MHz is needed, and where the internal reference frequency is 200 kHz, the desired N values will range from 4400 to 4575.

The charge pump output of the ADF4111 (Pin 2) drives the loop filter. This filter ($Z(s)$ in Figure 2) is basically a 1st-order lag-lead type. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45 degrees. Other PLL system specifications are given below:

K_D = 5 mA
K_V = 8.66 MHz/V
Loop Bandwidth = 12 kHz
F_{REF} = 200 kHz
N = 4500
Extra Reference Spur Attenuation = 10 dB

All of these specifications are needed and used to come up with the loop filter components values shown in Figure 6.

The loop filter output drives the VCO, which, in turn, is fed back to the RF input of the PLL synthesizer and also drives the RF Output terminal. A T-circuit configuration with 18-ohm resistors is used to provide 50-ohm matching between the VCO output, the RF output and the RF_{IN} terminal of the ADF4111.

In a PLL system, it is important to know when the system is in lock. In Figure 6, this is accomplished by using the MUXOUT signal from the ADF4111. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or *lock-detect* signal. When MUXOUT is chosen to select lock detect, it can be used in the system to trigger the output power amplifier, for example.

The ADF4111 uses a simple 4-wire serial interface to communicate with the system controller. The reference counter, the N counter and various other on-chip functions are programmed via this interface.

CONCLUSION

In this first part of the series, we have introduced the basic concepts of PLLs with simple block diagrams and equations. We have shown a typical example of where the PLL structure is used and given a detailed description of a practical implementation.

In the next installment, we will delve deeper into the specifications which are critical to PLLs and discuss their system implications.

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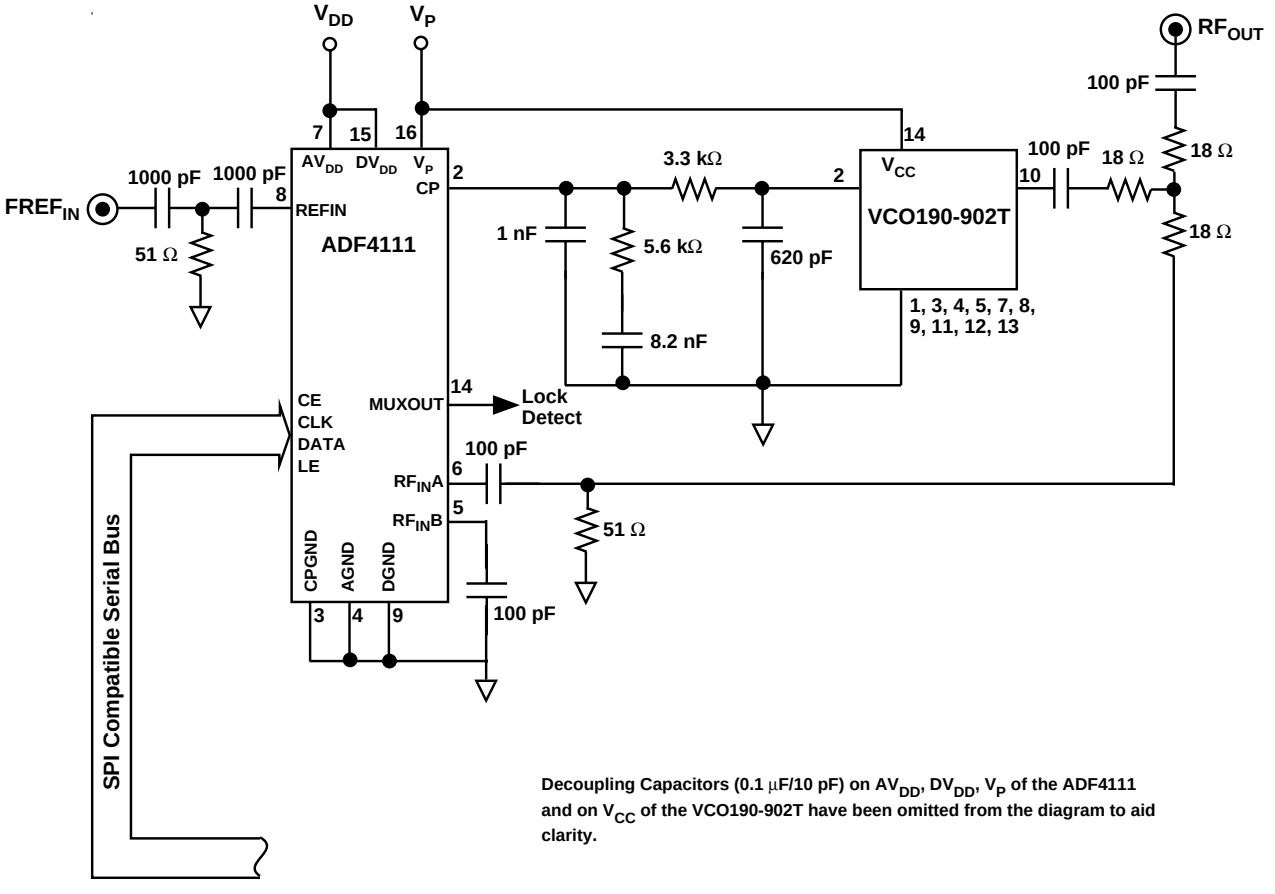

Figure 6. Transmitter local oscillator for GSM handset.