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Why Does Voltage Reference Noise Matter?

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There is increasing demand for ultrahigh precision measurements that can achieve greater than 24-bit resolution in industries from aerospace and defense and gas exploration to pharmaceutical and medical device manufacturers. For example, the pharmaceutical industry uses high precision lab balances that offer 0.0001 mg resolution over a 2.1 g full-scale range that would require an analog-to-digital converter (ADC) with greater than 24-bit resolution. Calibration and testing of these high precision system challenges the instrumentation industry to offer test equipment that can achieve greater than 25-bit resolution with at least 7.5 digit measurement precision.

To achieve this high resolution, a signal chain with exceptionally low noise is required. Figure 1 shows the relationship of noise vs. effective number of bits (ENOB) and signal-to-noise ratio (SNR). Note, noise is calculated based on voltage reference (V_{REF}) equal to 5 V and ADC input set to full-scale range. To provide perspective, to achieve 25-bit resolution, or 152 dB dynamic range, the maximum allowable system noise is 0.2437 µV rms.

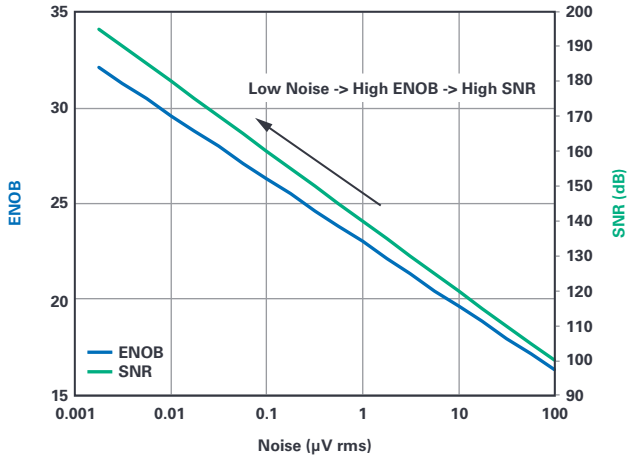

Figure 1. Noise vs. ENOB and SNR.

The voltage reference sets the limit to the input analog signal that the ADC can resolve. Equation 1 is the ideal transfer function of an ADC where the output code—in decimal form—is computed by the analog input signal V_{IN}, voltage reference V_{REF}, and number of ADC bits N.

$$ADC\ Code = V_{IN} \times \frac{2^N}{V_{REF}} \quad (1)$$

Typically, the resolution stated in the ADC data sheet is based on an input shorted technique where the ADC input is connected to the GND or the ADC differential inputs are connected to a common source. The ADC input shorted technique helps to characterize the absolute limit of the ADC resolution by omitting the ADC input source noise and eliminating the effect of V_{REF} noise. This is true because V_{IN} is set to 0 V, resulting in the ratio V_{IN}/V_{REF} being equal to 0 V.

To investigate the effects of voltage reference noise on overall system noise, Figure 2 shows the relationship between total system noise (rms) with ADC input dc source voltage. For this test, we used the AD7177-2 32-bit ADC with the V_{REF} input connected to the LTC6655-5 (5 V) and the ADC input connected to a low noise dc source. The ADC output data rate was set to 10 kSPS. Note, throughout the ADC input voltage range, the ADC noise remains constant (35 nV/$\sqrt{Hz}$) while the ADC dc input source noise rises (≤6 nV/$\sqrt{Hz}$) but remains low in comparison to the voltage reference noise (96 nV/$\sqrt{Hz}$). As shown in Figure 2, the total noise is proportional to the ADC dc input voltage. This is because as V_{IN} increases, the ratio V_{IN}/V_{REF} increases and so the V_{REF} noise dominates the overall system noise when the ADC is at full-scale input. The individual noise of each component in the signal chain adds together in root sum square (RSS) fashion and gives rise to the shape of the curve in Figure 2.

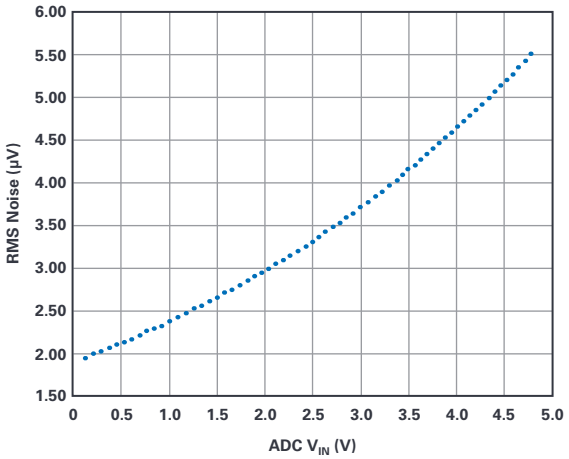

Figure 2. Relationship of ADC V_{IN} with rms system noise. V_{REF} set to LTC6655-5.

To achieve a high measurement resolution of 25 bits or beyond, even the best standalone voltage reference available in the market with a low noise specification needs some help to attenuate its noise. Adding external circuitry such as a filter can help attenuate noise to achieve the desired ADC dynamic range.

The remainder of this article explains various types of low-pass filters and how they can be applied to attenuate voltage reference noise. Filter design techniques and filter trade-offs will be discussed. Two types of low-pass filters that will be discussed in the context of attenuated voltage reference noise are simple passive RC low-pass filters (LPFs) and active-based signal flow graph (SFG) low-pass filters. System evaluation results using a sigma-delta (Σ-Δ) ADC will be presented in the circuit performance section.

Noise Reduction Using a Passive Low-Pass Filter

Figure 3 shows the voltage reference driving an ADC via a low-pass filter implemented with an external reservoir capacitor, C1, the equivalent series resistance (ESR) of the reservoir capacitor and the output impedance of voltage reference operational amplifier (op amp). The passive RC LPF cutoff frequency is determined by

$$f_C = \frac{1}{2\pi RC} \quad (2)$$

which states that bandwidth is inversely proportional to resistance R and capacitance C.

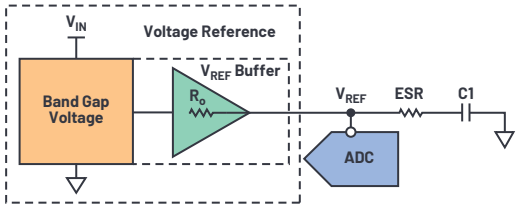

Figure 3. Low-pass filter between series voltage reference and ADC.

Reservoir capacitor C1 also works as local energy storage to compensate for voltage spikes caused when ADC voltage reference circuitry demands sudden change in load current. Figure 4 shows the sigma-delta AD7177-2 and SAR AD7980 ADC dynamic reference current response.

The user can choose the value of the C1 capacitor to meet the LPF cutoff frequency requirement, but some SAR ADCs require 10 µF minimum capacitor on the reference input in order to operate correctly. This minimum 10 µF C1 capacitor reduces the phase margin of the reference buffer. As the phase margin reduces, the buffer feedback is no longer negative.[1] The signals near the unity-gain crossover frequency are fed back in-phase with the incoming signals.[1] This causes the closed-loop response to introduce noise peak near the crossover frequency.[1] Since the bandwidth from the cutoff frequency (–3 dB point) reaches up to 16 MHz, the total integrated noise (rms) is dominated by the noise peak. Even though voltage reference reservoir capacitor C1 operates as a noise filter and compensates for voltage spikes, the caveat is the noise peak. Figure 5 shows the noise peak of the LTC6655 voltage reference introduced by reservoir capacitor C1. The noise peak magnitude is determined by the value of the reservoir capacitor and its ESR rating.

Most voltage references are designed with a complex output stage to drive a large load capacitance suitable for ADC reference circuitry. For example, the LTC6655 output stage is designed to be critically damped with a reservoir capacitance set to 10 µF. When the LTC6655's reservoir capacitance is set to a minimum of 2.7 µF and a maximum of 100 µF, noise peaking is introduced.

The equivalent series resistance of the V_{REF} output reservoir capacitance does mitigate the primary noise peak but introduces a secondary noise peak at 100 kHz and above. This can be explained by the fact that the ESR of the cap introduces a zero, which leads to improving phase margin and reducing primary noise peak. However, this zero combines with the inherent zero of the LTC6655 and creates secondary noise peaking. Note, the noise response in Figure 5 is only valid for the LTC6655 voltage reference.

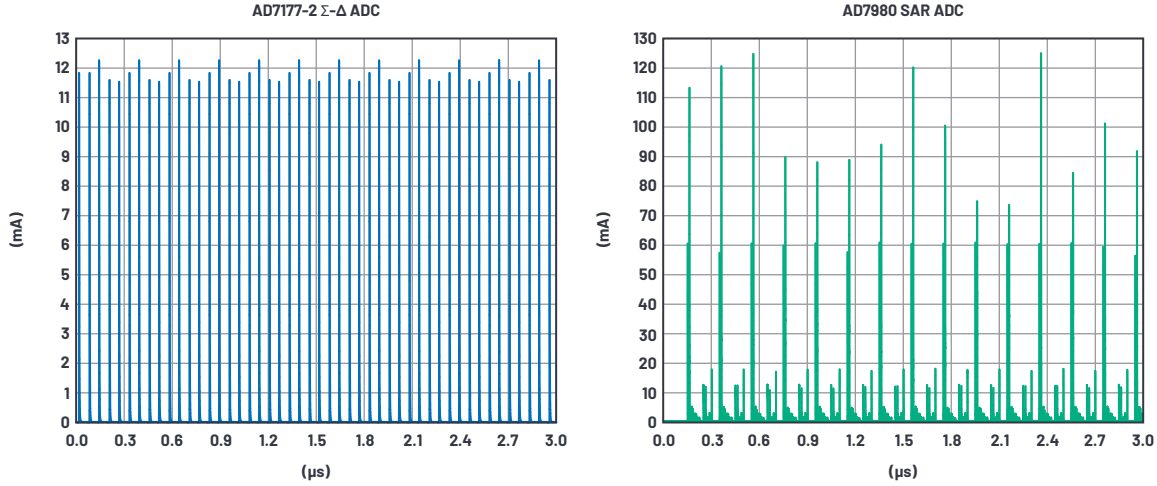

Figure 4. AD7177-2 and AD7980 simulated dynamic reference current response.

One of the other solutions to filter voltage reference noise, remove the noise peak, and properly drive the ADC is to add a passive RC LPF followed by a buffer. By adding a buffer, we separate the design constraints of the LPF and the ADC reference input capacitor. See Figure 6.

Setting the passive RC LPF cutoff frequency well below the unity-gain crossover frequency will not only reduce broadband and low frequency noise but also avoid noise peaking. For example, Figure 7 shows the LTC6655 noise response with C1 = 100 µF (ESR = 0 Ω), followed by a passive LPF where R = 10 kΩ and C2 = 10 µF (ESR = 0 Ω), creating a pole at 1.59 Hz.

Increasing the low-pass filter resistor R can help achieve a low cutoff frequency, but can also result in dc accuracy degradation of precision voltage reference. When adding a passive RC LPF, the user must also consider the impact on the load regulation and the impact on the V_{REF} buffer response (τ = RC), which affects its transient performance when driving an ADC.

To achieve the required transient performance, it is suggested to use a buffer as shown in Figure 6. Critical specifications to consider in terms of selecting buffer includes ultralow noise, capability to support high load capacitance, low distortion, excellent slew rate, and wide gain bandwidth. Recommendations for reference buffers are the ADA4805-1 and ADA4807-1.

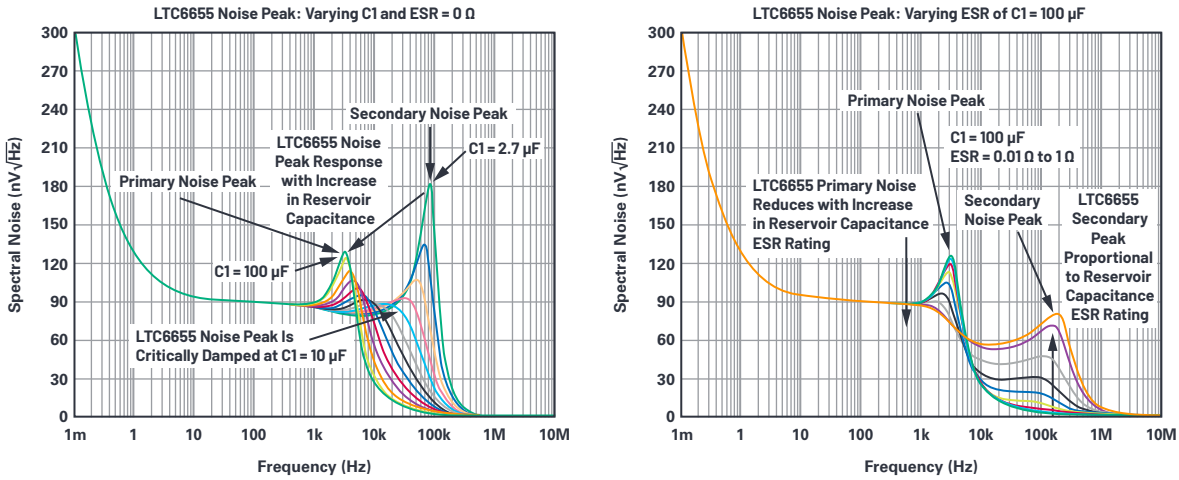

Figure 5. LTC6655 voltage reference noise peaking density.

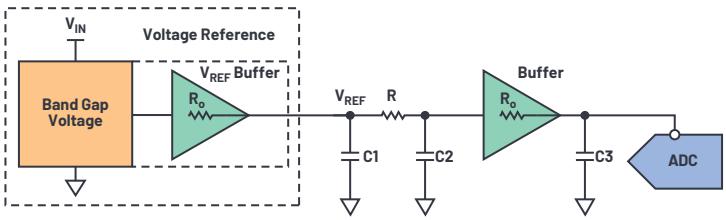

Figure 6. Passive RC LPF followed by a buffer.

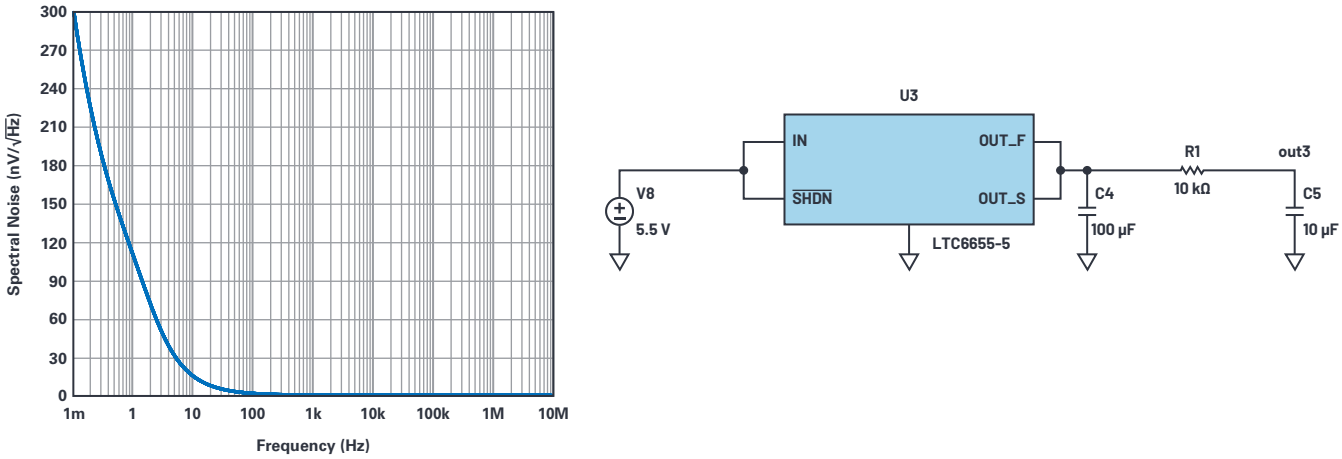

Figure 7. LTC6655-5 followed by passive RC LPF noise response.

Noise Reduction Using an Active LPF

Table 1 states the required dynamic range and maximum allowable system noise that must be met in order to achieve the desired ENOB ADC resolution. Depending on the ADC bandwidth, a single-pole, low-pass filter attenuating at 20 dB/decade may not achieve the desired wideband noise reduction. Cascading passive low-pass filters creates a ladder structure that can generate a higher order filter, but each section's input impedance will be a load on the previous section. This can degrade the dc accuracy of the precision voltage reference. However, designing a higher order LPF based on active components will provide excellent isolation between input to output, minimizing voltage reference dc accuracy degradation, and provide low output impedance to drive the reference circuitry of the ADC.

$$SNR = 6.02N + 1.76 \text{ dB} \quad (3)$$

$$LSB = \frac{V_{REF}}{2^N} \quad (4)$$

Table 1. Condition: V_{REF} = 5 V and ADC Input Set to Full-Scale Range

ENOB	SNR (dB)	Noise (µV rms)
20	122.16	7.798301
21	128.18	3.89942
22	134.2	1.949845
23	140.22	0.97499
24	146.24	0.487528
25	152.26	0.243781
26	158.28	0.121899
27	164.3	0.060954
28	170.32	0.030479
29	176.34	0.015241
30	182.36	0.007621
31	188.38	0.003811
32	194.4	0.001905

There are several different types of active low-pass filters—for example, Bessel, Butterworth, Chebyshev, and elliptic—as shown in Figure 8. Having a band-pass that is flat or does not exhibit ripple will keep the precision voltage reference's dc accuracy degradation to a minimum. Out of all filter types, designing LPF based on the Butterworth topology can achieve flat band-pass and steep attenuation.

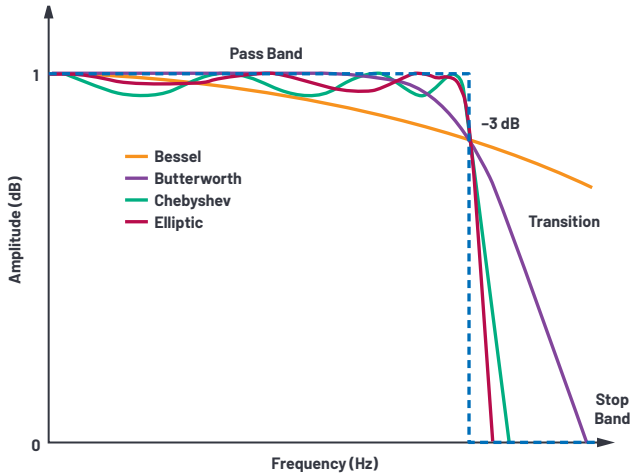

Figure 8. Filter amplitude response examples.

Active Low-Pass Filter Design Technique

A signal flow graph is a graphical representation of a system derived from a set of linear equations.[2] An SFG provides a bridge from a transfer function to a corresponding circuit topology of a system.[2] This theory can be applied to designing analog filters based on active circuitry. The key advantage of an SFG filter design approach is that the damping factor, Q, and cutoff frequency can be individually controlled. An SFG LPF can help to attenuate noise and improve SNR, but comes at the cost of additional bill of material (BOM) expenses, PCB area, and power. Furthermore, an SFG LPF can affect the reference output voltage with temperature leading to a small PPM error and hence dc accuracy degradation. Figure 9 shows an example of second-order low-pass filter transitioning from transfer function to circuit blocks via the SFG method. The scaling resistor (R) and capacitor (C) configures for the cutoff frequency (please see Equation 5).

For more details about signal flow graph theory, please refer to *Feedback Control of Dynamic Systems*, published by Addison-Wesley.[2]

$$R = Rs \times Rn \qquad C = \frac{Cn}{Ws \times R} \quad (5)$$

where

Rs is scaling factor

Cn is scaling factor

Ws is cutoff frequency (Rad/s)

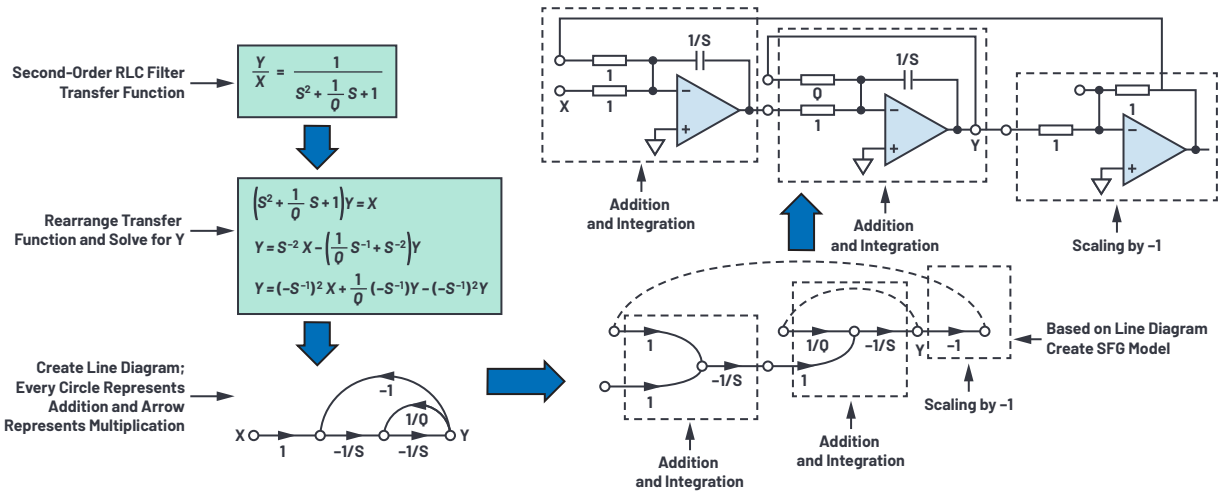

Figure 9. Active RC low-pass filter implementation based on SFG method.

The following is a calculation example for designing a second-order, 0.5 Hz cutoff frequency SFG low-pass Butterworth filter:

- For simplicity of this example, select Rs = 1 Ω, Cn = 1 F.
- Select Fs = 0.5 Hz to maximize rejection of broadband noise. Ws = 2 × π × 0.5 = 3.141 rad.
- Set the damping factor Q = 0.71. Select this value to achieve a flat band-pass and steep attenuation to reflect Butterworth topology.
- R, C, and Rq values were chosen based on an iterative process to achieve low thermal noise and the availability of component values for surface mount.

$$R = 7.32\ \text{k}\Omega$$

$$C = \frac{1}{2 \times \pi \times 0.5\ \text{Hz} \times 7.32\ \text{k}\Omega} = 44\ \mu\text{F} \quad (6)$$

$$Rq = R \times Q = 7.32\ \text{k}\Omega \times 0.71 = 5.2\ \text{k}\Omega$$

Introducing LTC6655LN

Considering the RC LPF and SFG LPF trade-offs, a better solution is to have a low-pass filter placed before the integrated low noise buffer of the voltage reference as shown in Figure 10. This implementation will not only reduce the PCB area but also not hinder the voltage reference buffer response. Using a voltage reference buffer with fast settling, high input impedance, and the capability to sink and source current will help overcome poor load regulation, maintain dc accuracy, and improve transient performance. The LTC6655LN takes advantage of this architecture. It comes with a noise reduction pin that enables reduction of wideband noise and an integrated output stage buffer. LTC6655LN is internally equipped with R3 resistor (see Figure 10) and allows users to connect external capacitor at the noise reduction (NR) pin to create a low-pass filter. With LTC6655LN architecture, users can configure the low-pass cutoff frequency based on their system requirements.

Table 2. The 3 dB Cutoff Frequencies for Different Values of the Capacitor Connected to the NR Pin

CNR	2.500	4.096	5.000	V
0.1 µF	5305	4233	3969	Hz
1 µF	531	423	397	Hz
10 µF	53	42.3	39.7	Hz
100 µF	5.3	4.2	4.0	Hz

The LTC6655LN RC LPF is connected to the noninverting node of the buffer, which is the most sensitive pin on this device. Precaution must be taken when selecting a low leakage type for the external capacitor to prevent leakage current flow through the R3 resistor, which can degrade dc accuracy. Furthermore, the variation of R and C do not track each other and therefore the RC time constant and LPF cutoff frequency can change due to process, voltage, and temperature (PVT) variation.

Table 3. Resistance Value of R3 for the Three Voltage Options

Voltage Option	2.500 V	4.096 V	5.000 V
R3 ± 15%	300 Ω	376 Ω	401 Ω

A voltage reference such as the LTC6655LN with an internally built-in LPF provides the best solution in simplifying noise filter design and eliminating the need for external buffer to drive ADC voltage reference circuitry.

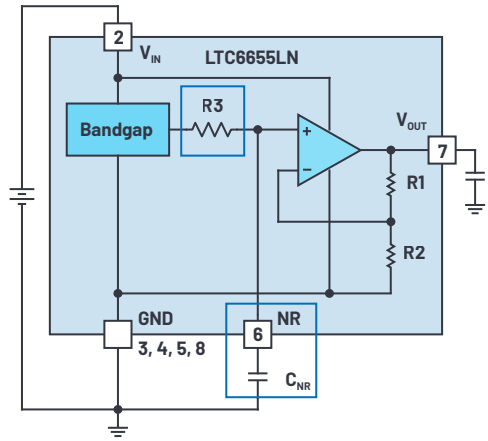

Figure 10. LTC6655LN block diagram.

Test Circuit Description

The AD7177-2 precision ADC was used to benchmark the performance of LTC6655/LTC6655LN with a 10 µF NR capacitor and LTC6655 followed by an active SFG filter. The AD7177-2 is a high resolution, 32-bit, low noise, fast settling, 2-channel/4-channel, sigma-delta, analog-to-digital converter for low bandwidth inputs. AD7177-2 is integrated with a programmable digital low-pass filter that allows users to control the output data rate (ODR) from 5 SPS to 10 kSPS.

The components used in designing SFG LPF (Figure 11) were two ADA4522-1 op amps, an AD797 op amp, 25 ppm surface-mount resistors, multilayer surface-mount ceramic capacitors, and a 10 µF WIMA film capacitor. ADA4522 is a rail-to-rail output op amp with a broadband noise density of 5.8 nV/√Hz and 177 nV p-p flicker noise. AD797 is a low noise op amp with 0.9 nV/√Hz broadband noise, 50 nV p-p flicker noise, excellent slew rate of 20 V/µs, and gain bandwidth of 100 MHz, which makes it suitable for driving an ADC.

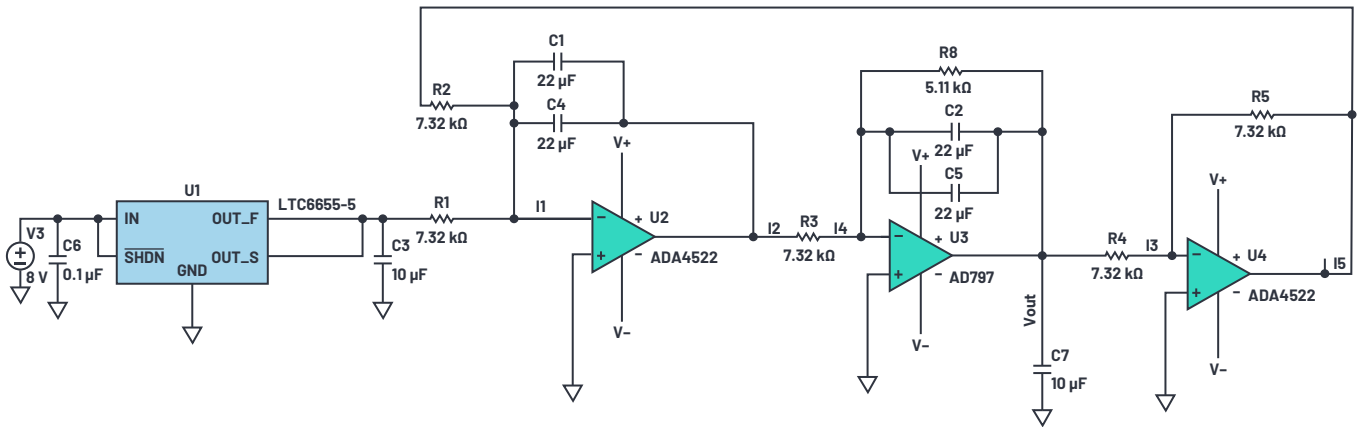

Figure 11. SFG LPF.

In order to correctly evaluate the performance when using an LTC6655 and an LTC6655LN with an AD7177-2, a dc source with overall noise lower than the ADC voltage reference and the ADC noise is required. Therefore, an ideal source was used, namely a 9 V battery supply as can be seen in Figure 12.

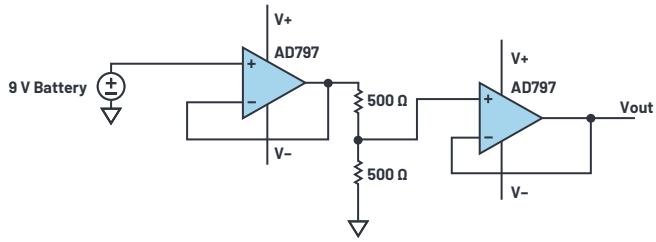

Figure 12. Low noise dc source.

Circuit Performance

Figure 13 displays spectral noise density and Figure 14 displays output data rate (ODR) vs. ENOB, depicting the performance of AD7177-2 with its V_{REF} input connected to a LTC6655/LTC6655LN with 10 µF NR capacitor or a filtered LTC6655 (SFG). To provide perspective of spectral noise density comparison at 1 kHz, see Table 4. Both Figure 13 and Figure 14 have two important regions.

Table 4. Spectral Noise Density Comparison at 1 kHz

	LTC6655	LTC6655LN with 10 µF NR Capacitance	LTC6655 SFG Filter	ADC Input DC Source
Spectral Noise Density at 1 kHz (nV/√Hz)	96	32	2.4	6.7

Region A:

Spectral noise density plot Figure 13 shows that at ODR of 500 SPS and higher, both the filtered LTC6655 (SFG) and ADC dc input source noise are significantly lower noise than the ADC. This results in the least amount of deviation from the maximum performance achievable by the ADC as shown in region A in Figure 14. The key takeaway based on ODR vs. ENOB and spectral noise density plot is that, within region A, the rise of the total integrated noise (rms) prevents the signal chain from achieving 25-bit measurement resolution.

Region B:

In this region, the spectral noise density plot (Figure 13) shows that the flicker noise of the three voltage reference options and the dc source increase and overall system noise are dominated by the dc source noise. This increase in flicker noise within region B explains the rise in deviation of ENOB between the measured performance and maximum achievable by the ADC (Figure 14).

According to ODR vs. ENOB plot, filtered LTC6655 (SFG) achieves 25-bit resolution at 20 SPS and lower while the LTC6655LN-5 with 10 µF NR cap and the LTC6655 cannot achieve better than 24.6-bit resolution.

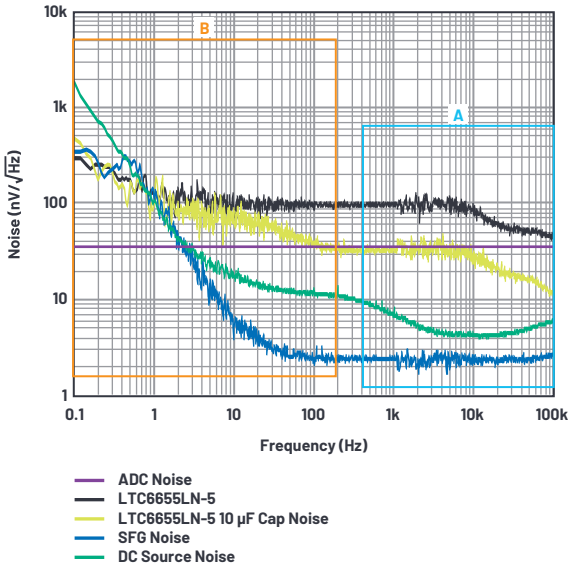

Figure 13. Spectral noise density.

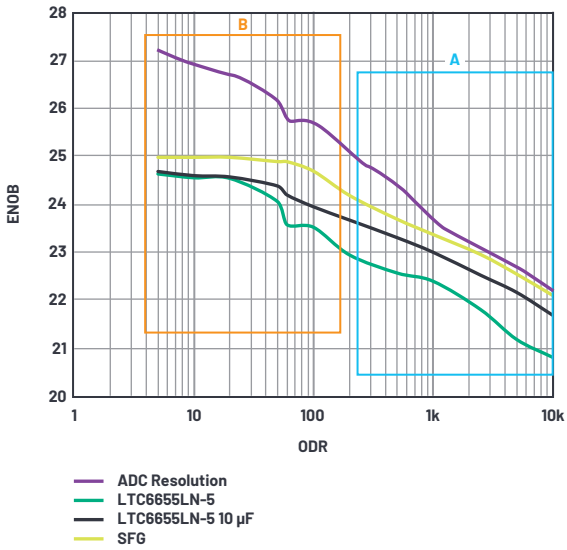

Figure 14. ODR vs. ENOB.

Table 5 below is a summary of the AD7177-2 ADC performance with the V_{REF} input either connected to a LTC6655/LTC6655LN with 10 µF NR capacitance or filtered LTC6655 (SFG). With ADC inputs tied together and the V_{REF} input connected to LTC6655, the zero-scale column establishes the best dynamic range AD7177-2 can achieve. With the ADC inputs nearly set to full-scale range, LTC6655LN-5 with 10 µF NR cap increases on average 4 dB dynamic range for up to 59.96 SPS compared to LTC6655. On the other hand, a filtered LTC6655 (SFG) achieves on average a 7 dB increment in dynamic range compared to LTC6655 for up to 59.96 SPS. The dynamic range delta does not vary much below 59.96 SPS and the variance is mainly due to the dominated low frequency flicker noise induced by the ADC input dc source.

Compared to LTC6655/LTC6655LN with 10 µF connected to NR pin reduces the broadband noise at 1 kHz by 62% and filtered LTC6655 (SFG) reduces broadband noise by 97%.

Conclusion

A precision system that is attempting to achieve a 25-bit resolution or higher must account for the significance of voltage reference noise. As shown in Figure 2, the contribution of V_{REF} noise to system noise is proportional to the utilization of the ADC's full-scale range. This article shows that adding a filter to a precision voltage reference attenuates V_{REF} noise, which leads to reducing overall system noise. An LTC6655 voltage reference followed by an SFG filter can reduce broadband noise by 97% of the LTC6655 with no filter. This comes at a cost of additional BOM, more PCB area, more power consumption, a few PPM of dc accuracy degradation, and can vary precision reference output with temperature. Considering SFG LPF trade-offs, LTC6655LN has leverage in terms of simple design, low power, only requires a single capacitor to reduce broadband noise, and eliminates the need for an external buffer to drive an ADC. LTC6655LN with 10 µF NR capacitor does reduce broadband noise by 62% of the LTC6655 with no filter. Hence, users can now take advantage of the built-in LTC6655LN low-pass filter to enable precision systems to achieve their desired resolution.

Addendum

To download LTspice®, please visit *analog.com/ltspice*.

Click here to download the LTspice simulation for the Figure 7 circuit, the SFG LPF circuit in Figure 11, and the low noise dc source circuit shown in Figure 12.

References

[1] Mark Reisiger. "Reduce Amplifier Noise Peaking to Improve SNR." *ElectronicDesign*, October 2012.

[2] Gene F. Franklin, J. David Powell, and Abbas Emami-Naeini. Feedback Control of Dynamics Systems. Addison-Wesley Longman Publishing Co., Inc., November 1993.

Acknowledgements

I would like to thank author Robert Kiely for his previous work on sigma-delta ADCs, precision amplifiers, and voltage references.

Table 5. Dynamic Range Comparison

ODR	ADC Dynamic Range Zero Scale (dB)	LTC6655 Dynamic Range (dB)	LTC6655LN 10 µF Dynamic Range (dB)	LTC6655 (SFG) Dynamic Range (dB)	Dynamic Range Delta (LTC6655LN 10 µF—LTC6655) (dB)	Dynamic Range Delta (LTC6655 (SFG)—LTC6655) (dB)
10000	135.40	126.88	132.22	134.65	5.33	7.77
5000	138.41	129.14	135.08	137.37	5.94	8.23
2500	140.82	132.91	137.23	139.86	4.32	6.95
1000	144.43	136.50	140.11	142.42	3.61	5.92
500	148.65	137.55	141.95	144.37	4.40	6.83
200	152.86	139.83	144.15	147.40	4.32	7.57
100	156.47	143.32	145.82	150.49	2.49	7.17
59.96	157.08	143.66	147.31	151.71	3.65	8.05
49.96	159.48	146.58	148.43	151.72	1.85	5.14
20	162.49	149.51	149.56	152.26	0.06	2.76
10	163.70	149.58	149.72	152.26	0.14	2.68
5	165.50	150.07	150.25	152.26	0.18	2.19

About the Author

Anshul Shah graduated from Arizona State University with an M.S. degree in electrical engineering. He is currently an applications engineer in ADI's Instrumentation and Precision Technology Group in Santa Clara, California, with a focus on precision voltage reference. Anshul joined Analog Devices in 2018. Prior to joining Analog Devices, Anshul held various positions in product test and validation at NXP Semiconductor. He can be reached at *anshul.shah@analog.com*.