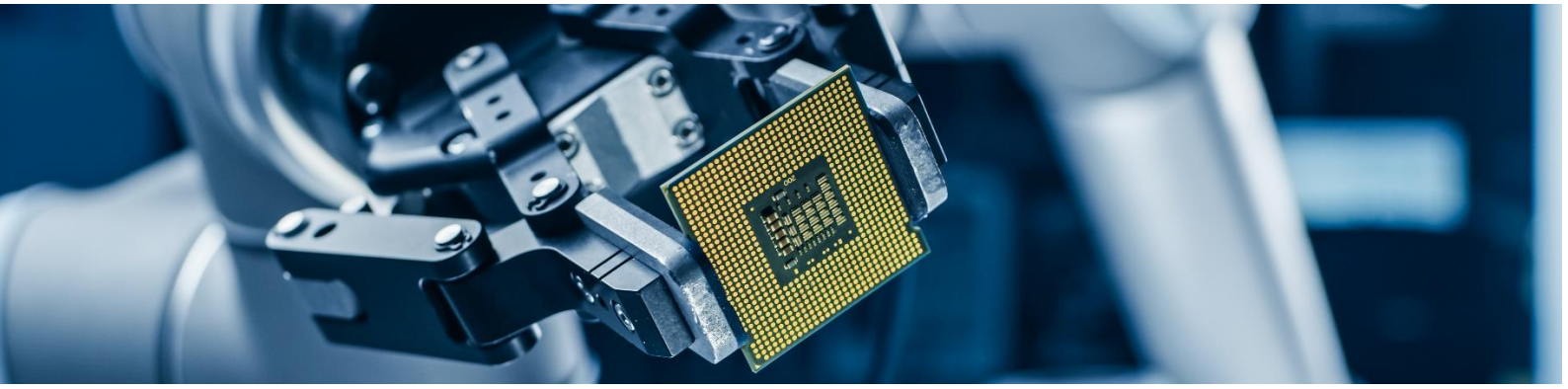
Event Invitation



Building Applications on multi-core RISC-V® based on Microchip PolarFire® SoC – Part I

Libero SoC and SoftConsole FPGA/Software Development Flow

13th October 2021 – online

Utilizing the flexibility and high level of integration provided by the PolarFire® SoC FPGA device family requires a broad range of expertise. It stretches from RTL development of IP cores for custom interfaces and accelerators and their integration into a system on the hardware side. On the software side, device drivers and application software have to be developed.

This webinar highlights the hardware related parts of the development process.

The webinar starts with a short overview of the PolarFire® SoC FPGA architecture. It proceeds with more details on the hardware specific parts that are different between different systems based on this SoC. An overview of the M100PFS SOM features and a minimal FPGA reference design illustrate these points. A simple custom GPIO and counter IP blocks are created and integrated into the system to demonstrate the development flow.

Compilation of the HSS (Hardware Software Services, zero-stage bootloader) sources and programming of the FPGA, HSS, and precompiled software images into the SoC concludes the webinar. The system can boot to U-Boot and custom IP blocks are exercised interactively with simple memory read and write commands.

All the details of the software boot process, device driver development and integration with a build system (we will use Yocto as an example) will be demonstrated in the second part of this webinar on November 10th 2021.

Speakers: Martin Kellermann (Microchip), Anton Kuzmin (ARIES Embedded)
Language: English
Prerequisites: None
Seminar Actions: Presentation
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Agenda (Time zone: CEST)

09:00 – 09:10	Welcome
09:10 – 09:30	Introduction to Microchip's PolarFire® SoC family
09:30 – 10:20	Designing IPs for Microchip's PolarFire® SoC with Libero SoC and SoftConsole
10:20 – 10:30	Questions & Answers

Register